1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K22

REV	ECN	DESCRIPTION OF REVISION	CK APPD
A	0000774858	PRODUCTION RELEASED	2009-08-21

LAST_MODIFIED=Thu Aug 20 17:40:45 2009

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5	6	Power Conn / Alias	MASTER	N/A
6	7	HOLES & STANDOFFS	MASTER	N/A
7	8	UNUSED SIGNAL ALIAS	MASTER	N/A
8	9	SIGNAL ALIASES	MASTER	N/A
9	10	CPU FSB	MASTER	N/A
10	11	CPU TEST & MISC.	MASTER	N/A
11	12	CPU POWER, GND, DECAPS	MASTER	N/A
12	13	eXtended Debug Port (XDP)	MASTER	N/A
13	14	MCP CPU Interface	MASTER	N/A
14	15	MCP Memory Interface	MASTER	N/A
15	16	MCP MEMORY CNTRL & MISC	MASTER	N/A
16	17	MCP PCIe Interfaces	MASTER	N/A
17	18	MCP Ethernet & Graphics	MASTER	N/A
18	19	MCP PCI & LPC	MASTER	N/A
19	20	MCP SATA & USB	MASTER	N/A
20	21	MCP HDA & MISC	MASTER	N/A
21	22	MCP Power & Ground	MASTER	N/A
22	25	MCP Standard Decoupling	K51	12/08/2008
23	26	MCP Graphics Support	MASTER	N/A
24	28	SB Misc	MASTER	N/A
25	29	FSB/DDR3 Vref Margining	MASTER	MASTER
26	30	MEMORY CAPS	MASTER	N/A
27	31	DDR3 SO-DIMMs 0 & 2	MASTER	N/A
28	32	DDR3 SO-DIMM CONNECTOR B	MASTER	N/A
29	33	DDR3 SUPPORT AND BITSWAPS	K51	10/13/2008
30	34	PCI-E Wireless Connector	MASTER	N/A
31	37	Ethernet PHY (RTL8211CL)	K51	12/08/2008
32	38	Ethernet Support	MASTER	N/A
33	39	ETHERNET CONNECTOR	MASTER	N/A
34	41	FireWire LLC/PHY (XIO2213B)	MASTER	N/A
35	42	FW: 1394B MISC	MASTER	N/A
36	43	FIREWIRE CONNECTOR	MASTER	N/A
37	45	SATA Connectors	MASTER	N/A
38	46	EXTERNAL USB CONNECTORS	MASTER	N/A
39	47	Internal USB Connections	MASTER	MASTER
40	49	SMC	MASTER	N/A
41	50	SMC Support	MASTER	N/A
42	51	LPC+SPI Debug Connector	MASTER	N/A
43	52	SMBUS CONNECTIONS	MASTER	N/A
44	53	CPU/MXM CURRENT AND VOLTAGE SENSE	MASTER	N/A
45	54	MCP CURRENT AND VOLTAGE SENSE	K51	12/08/2008
46	55	Thermal Sensors	MASTER	N/A
47	56	HD AND OD FAN	MASTER	N/A
48	57	CPU FAN	MASTER	N/A
49	61	SPI ROM	K51	12/08/2008
50	62	AUDIO: CODEC/REGULATOR	SKIPAUDIO	06/01/2009
51	63	AUDIO: FILTER/BUFFER	SKIPAUDIO	06/01/2009
52	64	AUDIO: SPEAKER AMP	SKIPAUDIO	06/01/2009
53	65	AUDIO: SPEAKER AMP	SKIPAUDIO	06/01/2009
54	66	Audio: MLB to I/O Conn.	SKIPAUDIO	06/01/2009
55	67	AUDIO: Detects/Grounding	SKIPAUDIO	06/01/2009
56	68	AUDIO: Mikey	SKIPAUDIO	06/01/2009
57	69	POWER SEQUENCING BLOCK DIAGRAM	K51	12/08/2008
58	70	PGOOD and Power Sequencing	MASTER	N/A
59	71	VREG: PPVCORE_S0_CPU	MASTER	N/A
60	72	VREG: PPVCORE_S0_CPU	MASTER	N/A
61	73	5V_S3 REGULATOR	MASTER	N/A
62	74	MCP CORE REGULATOR	MASTER	N/A
63	75	1.5V DDR SUPPLY	MASTER	N/A
64	76	FSB VTT/3.3V S5 SUPPLIES	MASTER	N/A
65	78	S3 & S0 FETs	MASTER	N/A
66	79	1V1 S5 POWER SUPPLY	K51	10/31/2008
67	80	1V8 POWER SUPPLY	MASTER	N/A
68	84	MXM PCIe, DP & Power	K51	10/31/2008
69	85	MXM I/O	K51	10/31/2008
70	86	MXM PCIE CAPS	MASTER	N/A
71	87	MXM ALIASES	MASTER	N/A
72	89	LCD MUX & CHOKES	MASTER	MASTER
73	90	INTERNAL DISPLAY	MASTER	MASTER
74	91	DP MUX SUPPORT	MASTER	N/A
75	93	DISPLAYPORT SUPPORT	MASTER	N/A
76	94	DisplayPort Connector	MASTER	N/A
77	100	CPU/FSB Constraints	MASTER	N/A
78	101	Memory Constraints	MASTER	N/A
79	102	MCP Constraints 1	MASTER	N/A
80	103	MCP Constraints 2	MASTER	N/A
81	104	Ethernet Constraints	MASTER	N/A
82	105	FireWire Constraints	MASTER	N/A
83	106	SMC Constraints	MASTER	N/A
84	107	GRAPHICS CONSTRAINTS	MASTER	N/A
85	108	K22/K23 SPECIFIC CONSTRAINTS	MASTER	N/A
86	109	K22/K23 RULE DEFINITIONS	MASTER	N/A
87	110	K22/K23 ICT/FCT	MASTER	N/A

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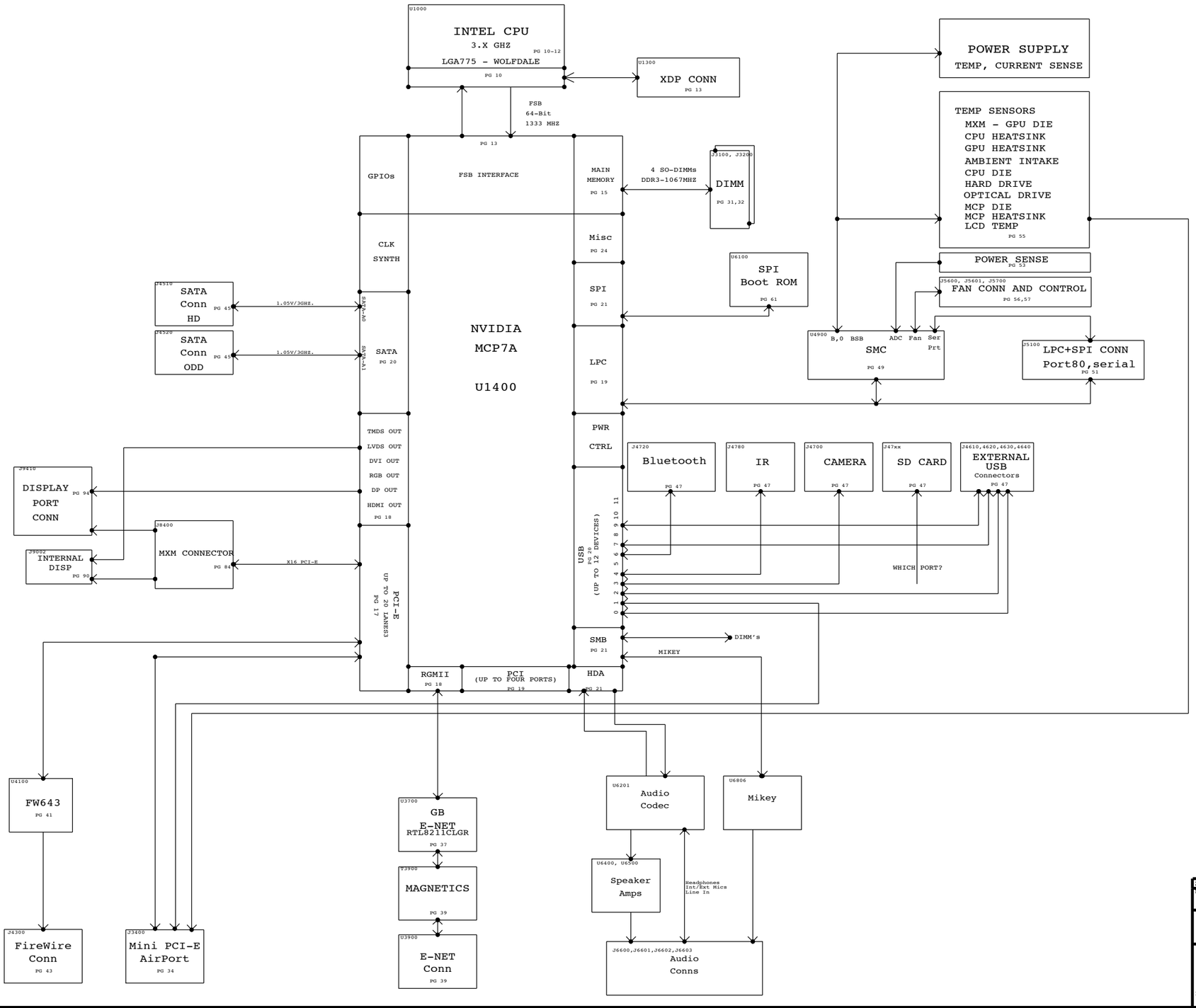

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System Block Diagram

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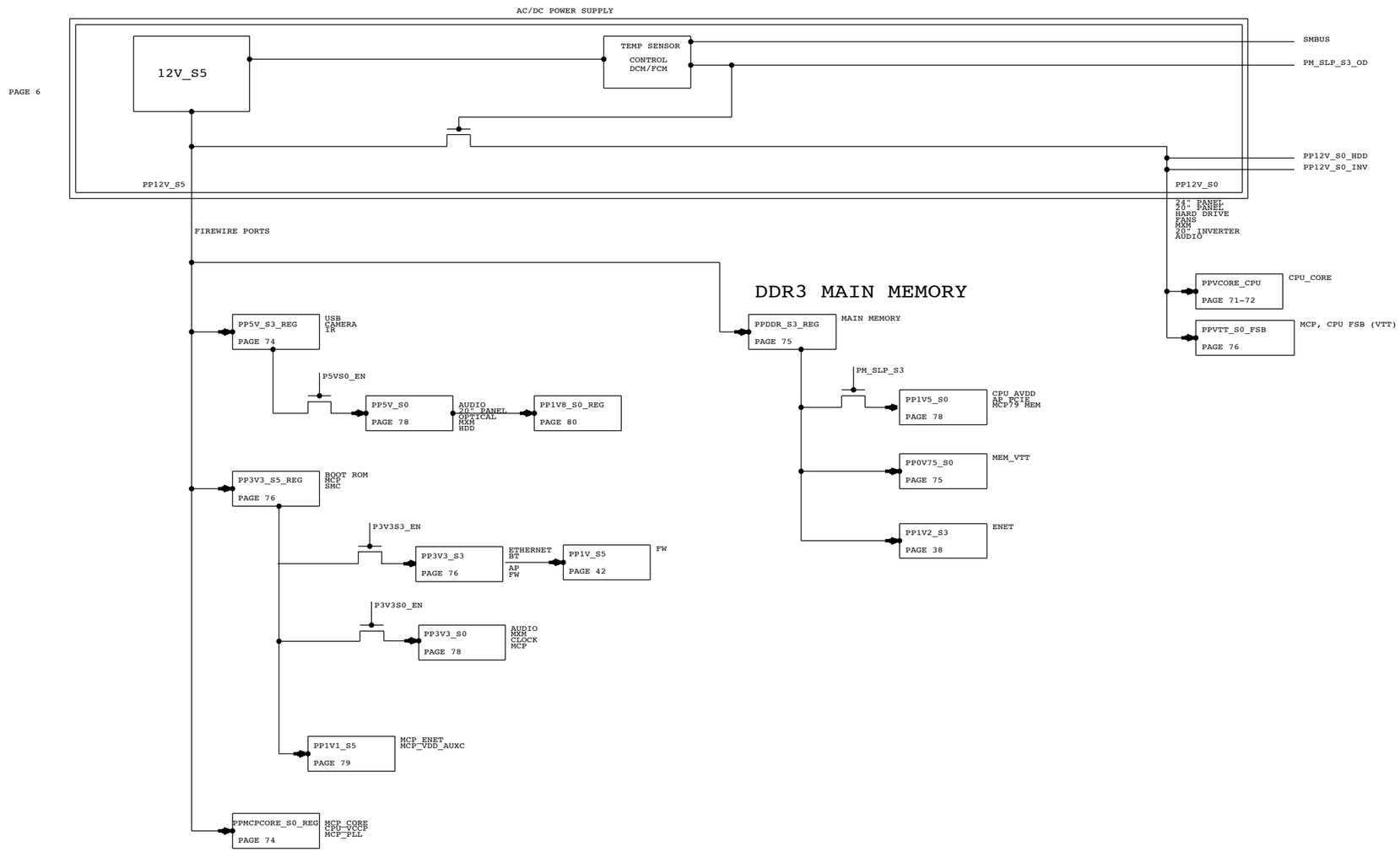

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Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9768	PCBA,MLB,GOOD,K22	K22,2P80GHZ_CPU,BASIC,IG
639-0036	PCBA,2.8 GHZ CPU,MXM,K22	K22,2P80GHZ_CPU,BASIC,MXM,K22_MXM
639-0184	PCBA,2.93 GHZ CPU,IG,K22	K22,2P93GHZ_CPU,BASIC,IG
639-0186	PCBA,2.93 GHZ CPU,MXM,K22	K22,2P93GHZ_CPU,BASIC,MXM,K22_MXM
639-0037	PCBA,3.0 GHZ CPU,IG,K22	K22,3P0GHZ_CPU,BASIC,IG
630-9878	PCBA,MLB,CTO,K22	K22,3P0GHZ_CPU,BASIC,MXM,K22_MXM
639-0183	PCBA,3.06 GHZ CPU,IG,K22(Investigation)	K22,3P06GHZ_CPU,BASIC,IG
639-0324	PCBA,MLB,3.16GHZ,MXM,K22	K22,3P16GHZ_CPU,BASIC,MXM,K22_MXM
639-0206	PCBA,MLB,3.33GHZ,IG,K22	K22,3P33GHZ_CPU,BASIC,IG
639-0207	PCBA,MLB,3.33GHZ,MXM,K22	K22,3P33GHZ_CPU,BASIC,MXM,K22_MXM
639-0392	PCBA,2.8 GHZ-2M CPU,IG,K22	K22,2P80GHZ_2M_CPU,BASIC,IG
639-0393	PCBA,2.8 GHZ-2M CPU,MXM,K22	K22,2P80GHZ_2M_CPU,BASIC,MXM,K22_MXM
607-4426	PCBA,MLB,DEV,K22	DEVELOPMENT,DEV_GROUP

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,MCP7A,XDP,BETTER,MCP_ISL9563A,MLB_PNL_PWR,PRODUCTION
MCP7A	BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP
DEV_GROUP	XDP_CONN,LPCPLUS,VREFMRGN,MCP_PWR_SENSE,MCP_CPU_TDIODE,PECI_SMB,MOJOMUX

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0731	1	IC,GMCP,MCP7A-JA,B03,35X35MM,BGA1437,DT	U1400	CRITICAL	IG
338S0732	1	IC,MCP,MCP7A-DA,B03,35X35MM,BGA1437,DT	U1400	CRITICAL	MXM
341T0170	1	IC,EFI BOOTROM,K22/K23	U6100	CRITICAL	
338S0765	1	IC,XIO2211ZAY,1394B,167BGA	U4100	CRITICAL	
338S0694	1	IC,RTL8251CA,GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

MCP -J SKU HAS INTEGRATED GPU
MCP -D SKU DOES NOT

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3745	1	WLF,QXXX,QS,2.80G,65W,1066,R0,3M,LGA	CPU	CRITICAL	2P80GHZ_CPU
337S3742	1	WLF,SLB9J,PRQ,2.83G,65W,1333,E0,6M,LGA	CPU	CRITICAL	2P83GHZ_CPU
337S3726	1	WLF,SLB9J,PRQ,3.0G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P0GHZ_CPU
337S3715	1	WLF,SLB9K,PRQ,3.16G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P16GHZ_CPU
337S3727	1	WLF,SLB9L,PRQ,3.33G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P33GHZ_CPU
337S3807	1	WLF,SLB9L,PRQ,2.93G,65W,1333,E0,6M,LGA	CPU	CRITICAL	2P93GHZ_CPU
337S3766	1	WLF,SLB9L,PRQ,3.06G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P06GHZ_CPU
337S3804	1	WLF,SLGU9,PRQ,2.80G,65W,1066,R0,2M,LGA	CPU	CRITICAL	2P80GHZ_2M_CPU

K22 PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7845	1	SCH,K22,MLB	SCH1		K22
	820-2494	1	PCBF,K22,MLB	MLB1		K22
(338S0563 - BLNK)	341T0168	1	IC,SMC,K22	U4900	CRITICAL	K22

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0111	127S0060		C6211	AUDIO, NEED QUAL

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PAGE TITLE
BOM Configuration

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EMC: C600,C626,C627,C628,C629,C630,C631
PLACE AT J600.

518-0352
CRITICAL
J600
76833-0100
M-RT-TH

52 =SMB_ACDC_SCL
45 6 =PP5V_S0_SATA
6 PP12V_S5
90 LCD_PWM
=SMB_ACDC_SDA 52
PP12V_S0 4 70
LCD_BKL_ON 89 90

C623 10UF 20% 10V X5R 805
C631 0.001UF 10% 50V X7R 402
C627 0.001UF 10% 50V X7R 402
C626 0.001UF 10% 50V X7R 402
C630 0.001UF 10% 50V X7R 402
C624 10UF 20% 16V X5R-CERM 1210

PM_ACDC_PS_ON
Q610 2N7002 SOT23-HF1
70 50 49 9 PM_SLPS3_BUF2_L
C600 0.001UF 10% 50V X7R 402

110 78 4 PP3V3_S3
DEVELOPMENT
R600 1K 5% 1/16W MF-LF 402
ITS_ALIVE
DEVELOPMENT
LED605 GREEN-3.6MCD 2.0X1.25MM-SM

76 6 PP3V3_S5_REG
R601 1K 5% 1/16W MF-LF 402
ITS_PLUGGED_IN
LED601 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:1

110 78 6 PP3V3_S3
R602 1K 5% 1/16W MF-LF 402
CORE_VOLTAGES_ON_R
LED602 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:2
CORE_VOLTAGES_ON
Q602 2N7002 SOT23-HF1
70 ALL_SYS_PWRGD_R

78 6 PP3V3_S0
MXM
R604 1K 5% 1/16W MF-LF 402
GPU_PRESENT_R
MXM
LED604 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:3
GPU_PRESENT_DRAIN
MXM
Q604 2N7002 SOT23-HF1
9 MXM_GOOD

90 PP5V_LCD_CONN
R603 1.5K 5% 1/16W MF-LF 402
LCD_SHOULD_ON
LED603 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:4

"S0" RAILS

ONLY ON IN RUN

75 PPVTT_S0_DDR_LDO
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP0V75_S0_MEM_VTT_A 31
=PP0V75_S0_MEM_VTT_B 32
=PPVTT_S0_VTTCLAMP 78

72 71 PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_CPU 12

74 54 PPMCPCORE_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_MCP 22 25
=PP1V05_S0_MCP_AVDD_UF 25
=PP1V05_S0_MCP_PEX_DVDD 25 28
=PP1V05_S0_MCP_PLL_UF 25
=PP1V05_S0_MCP_SATA_DVDD0 20 28
=PP1V05_S0_MCP_HDMI_VDD_R 26

76 PPVTT_S0_FSB_REG
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVTT_S0_CPU 10 50 55 71
=PPVTT_S0_FSB_CPU 11 12
=PPVTT_S0_XDP 13
=PP1V05_S0_MCP_FSB 14 22 25

54 PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V5_S0_CPU_VCCPLL 12
=PP1V8R1V5_S0_MCP_MEM 16 25 30
=PP1V5_S0_AUD_DIG 62
=PP1V5_FWRS0_FWXIO 41

80 PP1V8_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3R1V8_S0_MCP_IFP_VDD_R 26
=PP1V8_S0_PGCMP 70

78 6 PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.10MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S0_FAN 56 57
=PP3V3_S0_MCP 21 22 25
=PP3V3_S0_MCP_VPLL_UF 26
=PP3V3_S0_MCP_GPIO 18 19 21
=PP3V3_S0_MCP_PLL_UF 25
=PPSPD_S0_MEM_A 31
=PPSPD_S0_MEM_B 32
=PP3V3_S0_VRD 71
=PP3V3_S0_AUDIO 62 64 65 66 67 68
=PP3V3R1V5_S0_MCP_HDA 21 25
=PP3V3_S0_SMBUS 52
=PP3V3_S0_SMC_LS 50 55
=PP3V3_S0_SMBUS_SMC_0_S0 52
=PP3V3_S0_SMBUS_SMC_B_S0 52
=PP3V3_S0_SMBUS_SMC_MGMT 52
=PP3V3_S0_DPCONN 94
=PP3V3_S0_TSENS 55
=PP3V3_S0_MXM 84 85
=PP3V3_S0_XDP 13
=PP3V3_S0_ODD 45
=PP3V3_S0_SATALED 45
=PP3V3_S0_SMC 50 53 54
=PP3V3_S0_PWRCTL 70
=PP3V3_S0_MCPTHMSNS 55
=PP3V3_S0_VIDEO 89 90
=PP3V3_FW_FWPHY 41 42 43
=PP3V3_FWRS0_FWXIO 41

110 78 PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5.0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S0_LPCPLUS 51
=PP5V_S0_AUDIO 62 68
=PP5V_S0_SATA 6 45
=PP5V_S0_MXM 84
=PP5V_S0_VRD 71
=PP5V_S0_DP_AUX_MUX 93
=PP5V_S0_ISENSE 53
=PP5V_S0_PWRCTL 80
=PP5V_S0_LCD 90

70 6 PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=AUDIO
MAX_NECK_LENGTH=3 MM
=PP12V_S0_FAN 56 57
=PP12V_S0_AUDIO_SPKRAMP 67
=PP12V_S0_VRD 70 71
=PPV_S0_MXM_PWR 53
=PPVIN_S0_PPVTT_FSB 76
=PPVIN_S0_MCPCORE 74

"S3" RAILS

ON IN RUN AND SLEEP

75 PPDDR_S3_REG
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PPDDR_MAX
MAX_NECK_LENGTH=3 MM
=PP1V5_S3_MEM_A 30 31 108
=PP1V5_S3_MEM_B 30 32 108
=PP1V5_S3_MEMRESET 33
=PPDDR_S3_S0FET 78
=PPDDR_S3_PGCMP 70

75 PPVTT_S3_DDR_BUF
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 mm
=PPVTT_S3_DDR_BUF 29

110 78 6 PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S3_MINI 34
=PP3V3_S3_BT 47
=PP3V3_S3_VREFMRGN 29
=PP3V3_S3_SDCARD 47
=PP3V3_S3_MCP_GPIO 21
=PP3V3_S3_SMC
=PP3V3_S3_SMBUS_SMC_A_S3 52
=PP3V3_S3_MCPREG 74

110 73 PP5V_S3_REG
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S3_DDRREG 30 75
=PP5V_S3_USB 46
=PP5V_S3_VTTCLAMP 78
=PP5V_S3_PWRCTL 70
=PP5V_S3_S0FET 78
=PP5V_S3_MCPREG 74
=PP5V_S3_CAMERA 47
=PP5V_S3_IR 47
=PP5V_S3_1V8 80

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

79 PP1V1_S5_REG
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V05_S5_MCP_VDD_AUXC 22 25
=PP1V1_S5_ENET_FET 38

76 6 PP3V3_S5_REG
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S5_MCP 22 25
=PP3V3_S5_MCP_GPIO 18 20
=PP3V3_S5_SMC 49 50
=PP3V3_S5_ROM 51 61
=PP3V3_S5_RTC_D 28
=PP3V3_S5_LPCPLUS 51
=PP3V3_S5_SMBUS_SMC_BSA 52
=PP3V3_S5_SMCUSBMUX 46
=PP3V3_S5_MEMRESET 33
=PP3V3_S5_P1V1S5 79
=PP3V3_S5_PWRCTL 70
=PP3V3_S5_S3FET 78
=PP3V3_S5_S0FET 78
=PP3V3_S5_ENET_FET 38

76 PP5V_S5_LDO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S5_AVREF 50

6 PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP12V_S5_FW 43
=PPVIN_S5_DDRREG 75
=PPVIN_S5_P3V3S5 76
=PPVIN_S5_P5VS3 73
=PP12V_S5_REG 76
=PP12V_S5_PWRCTL 38 70 78

GND RAILS

GND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=AUDIO
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
Power Conn / Alias

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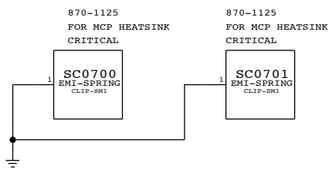
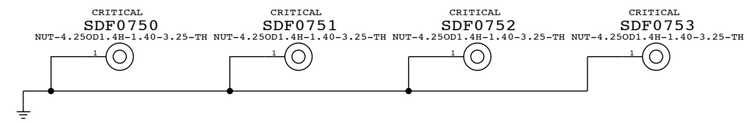
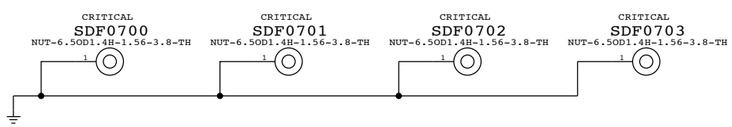


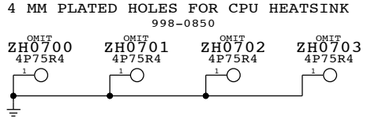
DIMM CONNECTOR NUTS



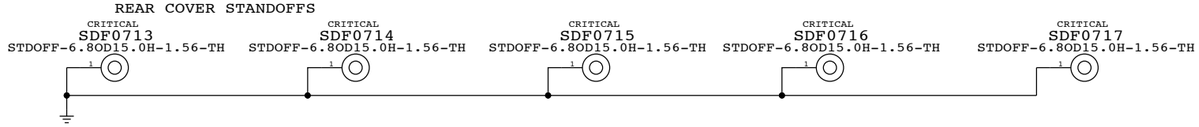
BACKER PLATE NUTS



4 MM PLATED HOLES FOR CPU HEATSINK



REAR COVER STANDOFFS



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PAGE TITLE
HOLES & STANDOFFS

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NC ON UNUSED ALIASES

18	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_MCP_RGB_HSYNC	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_MCP_RGB_VSYNC	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_AD<31..15>	NC_PCI_AD<31..15>	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_IRDY_L	NC_PCI_IRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_C_BE_L<1..0>	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_SERR_L	NC_PCI_SERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_DEVSEL_L	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_PERR_L	NC_PCI_PERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_LPC_DRQ0_L	NC_LPC_DRQ0_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_MCP_BUF_SIO_CLK	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE

18	TP_ENET_INTR_L	NC_ENET_INTR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_ENET_PWRDWN_L	NC_ENET_PWDWN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_MCP_KBDRSTIN_L	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
	TP_MCP_GPIO_18	NC_MCP_GPIO_18	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_MLB_RAM_SIZE	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_C_BE_L<3>	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_CLK0	NC_PCI_CLK0	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_CLK1	NC_PCI_CLK1	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_FRAME_L	NC_PCI_FRAME_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_GNT0_L	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_GNT1_L	NC_PCI_GNT1_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_INTW_L	NC_PCI_INTW_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_INTX_L	NC_PCI_INTX_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_INTY_L	NC_PCI_INTY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_INTZ_L	NC_PCI_INTZ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_RESET1_L	NC_PCI_RESET1_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_STOP_L	NC_PCI_STOP_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_TRDY_L	NC_PCI_TRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_PRSNT_L	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PE4_CLKREQ_L	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PE4_PRSNT_L	NC_PE4_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_SB_A20GATE	NC_SB_A20GATE	MAKE_BASE=TRUE	NO_TEST=TRUE
20	TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_MINI_N	NC_USB_MINI_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_MINI_P	NC_USB_MINI_P	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_EXCARD_N	NC_USB_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_EXCARD_P	NC_USB_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE
21	ODD_PWR_EN_L	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_P	NC_PCIE_CLK100M_EXCARD_P		NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_N	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	EXCARD_CLKREQ_L	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_AD<12..10>	NC_PCI_AD<12..10>	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_AD<8>	NC_PCI_AD<8>	MAKE_BASE=TRUE	NO_TEST=TRUE

17	TP_PCIE_PE4_R2D_CP	NC_PCIE_PE4_R2D_CP	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_PE4_R2D_CN	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_PE4_D2RP	NC_PCIE_PE4_D2RP	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_PE4_D2RN	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_D2R_P	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_D2R_N	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_P	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_N	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_TPAD_N	NC_USB_TPAD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_TPAD_P	NC_USB_TPAD_P	MAKE_BASE=TRUE	NO_TEST=TRUE

MCP HAS INTERNAL 15K PULL-DOWNS

UNUSED MEMORY SIGNALS

15	TP_MEM_A_CLK2P	NC_MEM_A_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE
15	TP_MEM_A_CLK2N	NC_MEM_A_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_A_CLK5P	NC_MEM_A_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_A_CLK5N	NC_MEM_A_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE
15	TP_MEM_B_CLK2P	NC_MEM_B_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE
15	TP_MEM_B_CLK2N	NC_MEM_B_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_B_CLK5P	NC_MEM_B_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_B_CLK5N	NC_MEM_B_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE

UNUSED GMUX JTAG FROM MCP

17	GMUX_JTAG_TCK_L	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	GMUX_JTAG_TDO	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE	NO_TEST=TRUE
19	GMUX_JTAG_TDI	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE	NO_TEST=TRUE
19	GMUX_JTAG_TMS	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE	NO_TEST=TRUE

SE=TRUE

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
UNUSED SIGNAL ALIAS

Apple Inc.

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SIGNAL ALIAS

21 TP_MLB_RAM_VENDOR — MXM_GOOD (MAKE_BASE=TRUE) 6

102 21 PM_SLP_S3_L — R910 15 (5% 1/16W MF-LF 402) — PM_SLPS3_BUF2_L (MAKE_BASE=TRUE) 6 49 50 70

(P50 HAS A 100K TO GROUND)

R911 15 (5% 1/16W MF-LF 402) — PM_SLPS3_BUF1_L (MAKE_BASE=TRUE) 73 94

R912 100K (5% 1/16W MF-LF 402)

46 20 USB_EXTC_OC_L (MAKE_BASE=TRUE)

46 USB_EXTD_OC_L

K22/K23 Use one GPIO for both ports 2&3 OC

USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD ITS OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

PEG Slot Support

17 IN	PEG_CLK100M_P	GPU_CLK100M_PCIE_P (MAKE_BASE=TRUE)	OUT 87 102
17 IN	PEG_CLK100M_N	GPU_CLK100M_PCIE_N (MAKE_BASE=TRUE)	OUT 87 102
17 IN	=PEG_R2D_C_P<0..15>	PEG_R2D_C_P<0..15> (MAKE_BASE=TRUE)	OUT 86 102
17 IN	=PEG_R2D_C_N<0..15>	PEG_R2D_C_N<0..15> (MAKE_BASE=TRUE)	OUT 86 102
17 OUT	=PEG_D2R_P<0..15>	PEG_D2R_P<0..15> (MAKE_BASE=TRUE)	IN 86 102
17 OUT	=PEG_D2R_N<0..15>	PEG_D2R_N<0..15> (MAKE_BASE=TRUE)	IN 86 102
17 IN	PEG_PRSNT_L	MXM_DETECT_L (MAKE_BASE=TRUE)	OUT 85

DisplayPort / TMDS Support

18 IN	=MCP_HDMI_TXC_P	DP_IG_ML_P<3> (MAKE_BASE=TRUE)	OUT 91 107
18 IN	=MCP_HDMI_TXC_N	DP_IG_ML_N<3> (MAKE_BASE=TRUE)	OUT 91 107
18 IN	=MCP_HDMI_TXD_P<0..2>	DP_IG_ML_P<2..0> (MAKE_BASE=TRUE)	OUT 91 107
18 IN	=MCP_HDMI_TXD_N<0..2>	DP_IG_ML_N<2..0> (MAKE_BASE=TRUE)	OUT 91 107
18 IN	=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK (MAKE_BASE=TRUE)	OUT 93
18 BI	=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA (MAKE_BASE=TRUE)	BI 93
18 OUT	=MCP_HDMI_HPD	DP_IG_HPD (MAKE_BASE=TRUE)	IN 91

18 =DVI_HPD_GMUX_INT — HPLUG_DET2 (MAKE_BASE=TRUE) — R900 20K (5% 1/16W MF-LF 402)

MCP79 PCIe PRSNT# Straps

PCIE_FW_PRSNT_L OUT 17

PCIE_MINI_PRSNT_L OUT 17

Audio Mux aliasing

103 64 IN AUD_SPDIF_IN (MAKE_BASE=TRUE) — AUD_SPDIF_IN_CODEC OUT 62

this alias connects spdif directly from the I/O port to the codec
K23 uses a mux between the DP audio source and the audio in port

62 IN AUD_MUX_CNTRL — TP_AUD_MUX_CNTRL (MAKE_BASE=TRUE)

K23 Uses this to control the DP audio mux. K22 does not need this signal

Platform Reset Connections

LPC Reset (Unbuffered)

103 19 IN LPC_RESET_L — R981 33 (5% 1/16W MF-LF 402) — DEBUG_RESET_L OUT 51

PLACEMENT_NOTE=Place close to U1400

R983 33 (5% 1/16W MF-LF 402) — SMC_LRESET_L OUT 49

PLACEMENT_NOTE=Place close to U1400

PCIE Reset (Unbuffered)

17 IN PCIE_RESET_L

- R992 0 (5% 1/16W MF-LF 402) — FW_RESET_L OUT 41
- R991 0 (5% 1/16W MF-LF 402) — MINI_RESET_L OUT 34
- R990 0 (5% 1/16W MF-LF 402) — PEG_RESET_L OUT 87 90
- R971 0 (5% 1/16W MF-LF 402) — PCA9557D_RESET_L OUT 29
- R993 0 (5% 1/16W MF-LF 402) — CARDREADER_PLT_RST_L OUT 47

19 IN MEM_VTT_EN_R — R972 33 (5% 1/16W MF-LF 402) — DDRVTT_EN OUT 75 78

NO STUFF
C973 0.47UF (10% 6.3V CERM-X5R 402)

103 19 IN LPC_CLK33M_SMC_R — R925 33 (5% 1/16W MF-LF 402) — LPC_CLK33M_SMC OUT 49 103

PLACEMENT_NOTE=Place close to U1400

R926 33 (5% 1/16W MF-LF 402) — LPC_CLK33M_LPCPLUS OUT 51 103

PLACEMENT_NOTE=Place close to U1400

103 21 IN PM_CLK32K_SUSCLK_R — R929 22 (5% 1/16W MF-LF 402) — PM_CLK32K_SUSCLK OUT 49 103

PLACEMENT_NOTE=Place close to U1400

MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP

21 IN MCP_CPUVDD_EN — R930 22 (5% 1/16W MF-LF 402) — MCP_CPU_VLD OUT 21

PLACEMENT_NOTE=Place close to U1400

18 =MCP_MII_RXER
18 =MCP_MII_COL
18 =MCP_MII_CRS

— MCP_MII_NU (MAKE_BASE=TRUE) — R955 47K (5% 1/16W MF-LF 402)

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: SIGNAL ALIASES

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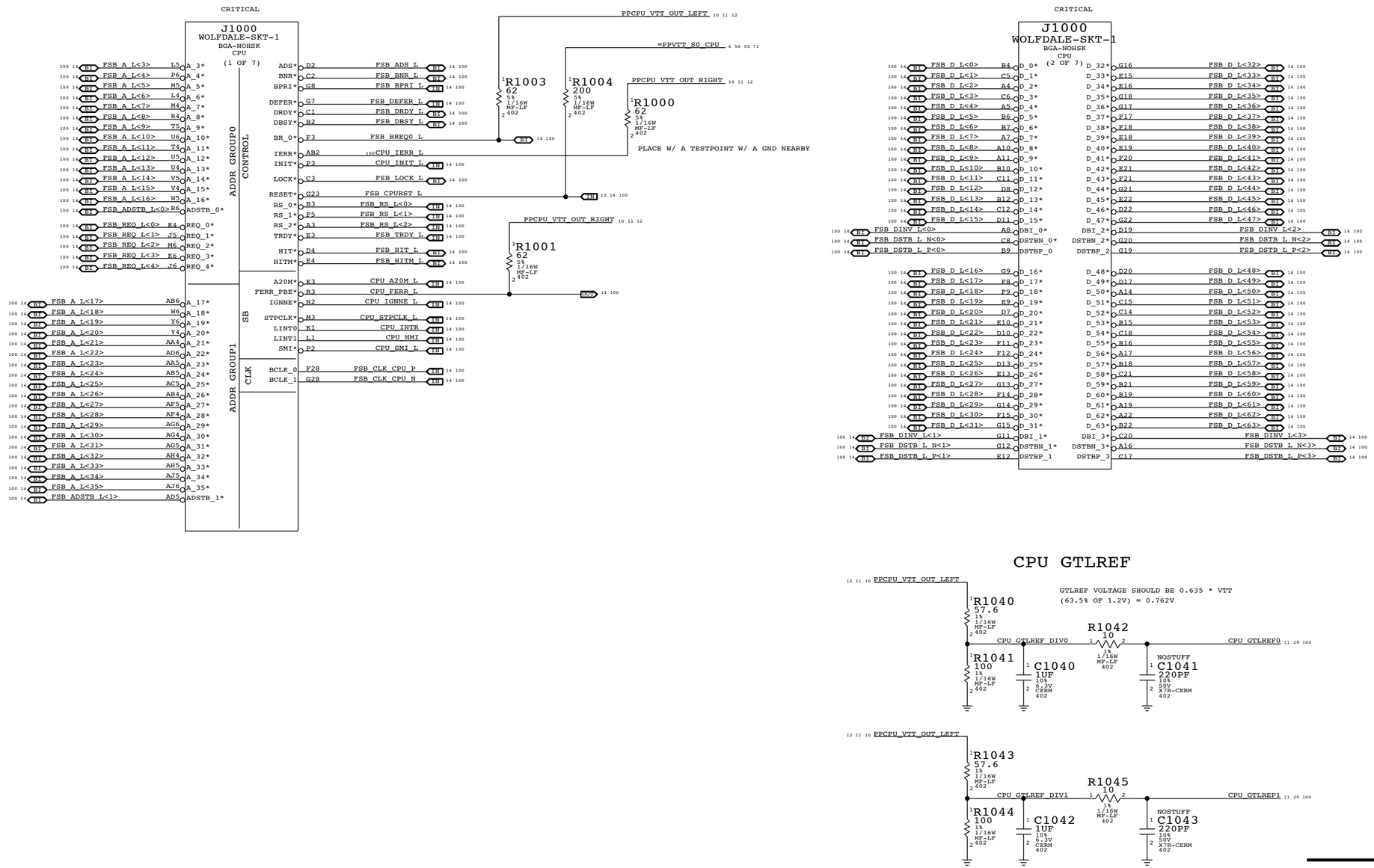

CPU GTLREF

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PAGE TITLE

CPU FSB

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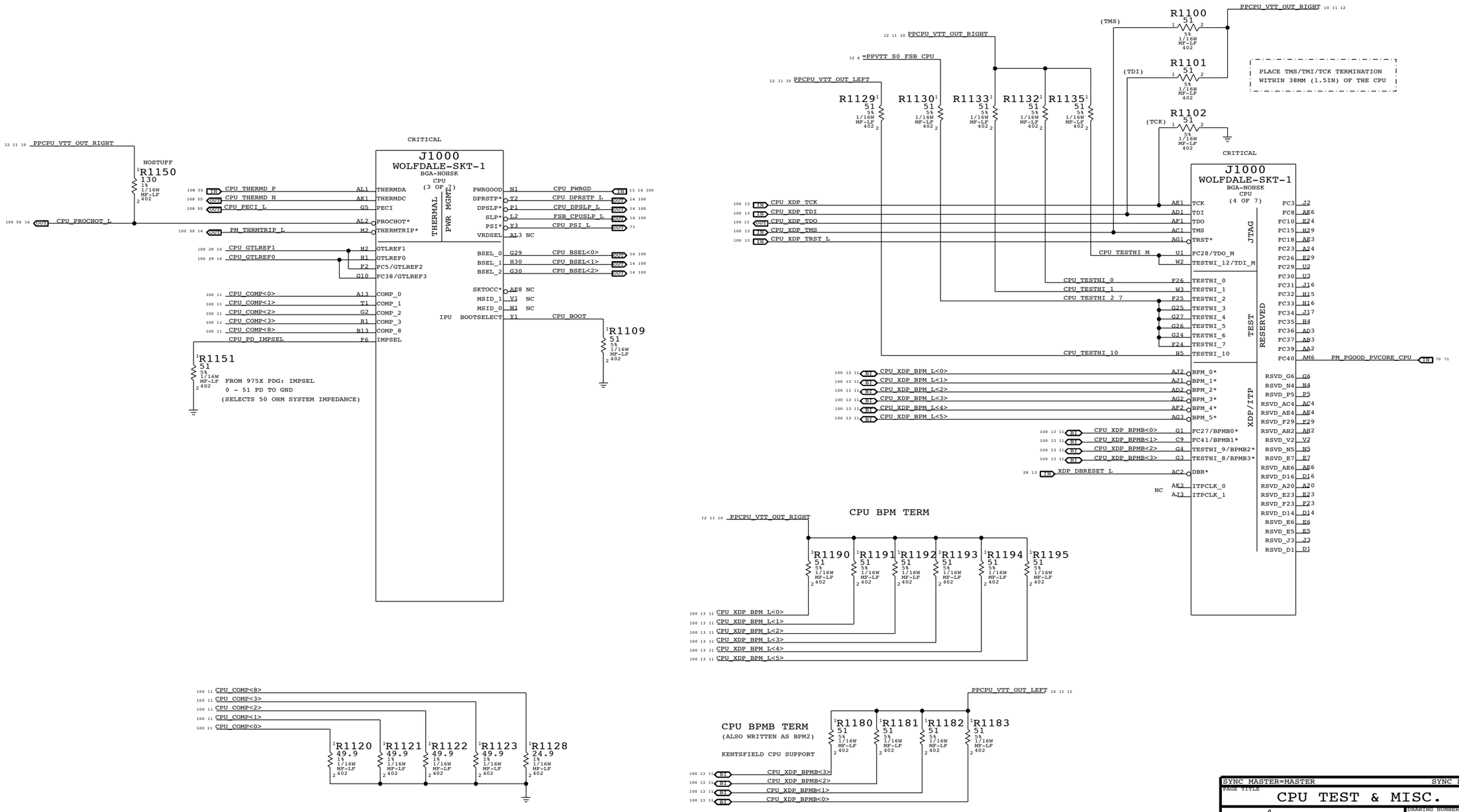

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PAGE TITLE

CPU TEST & MISC.

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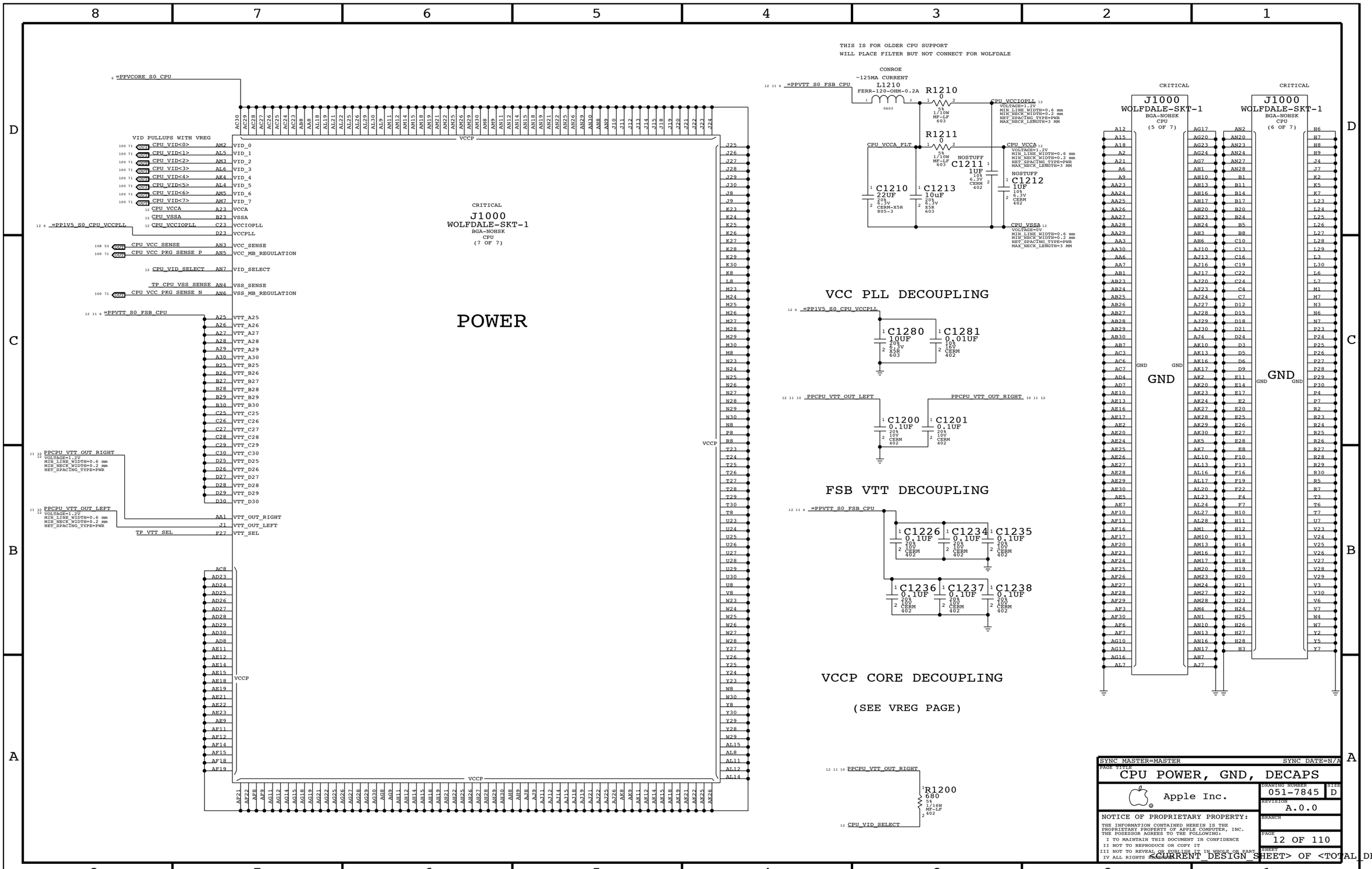

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PAGE TITLE

CPU POWER, GND, DECAPS

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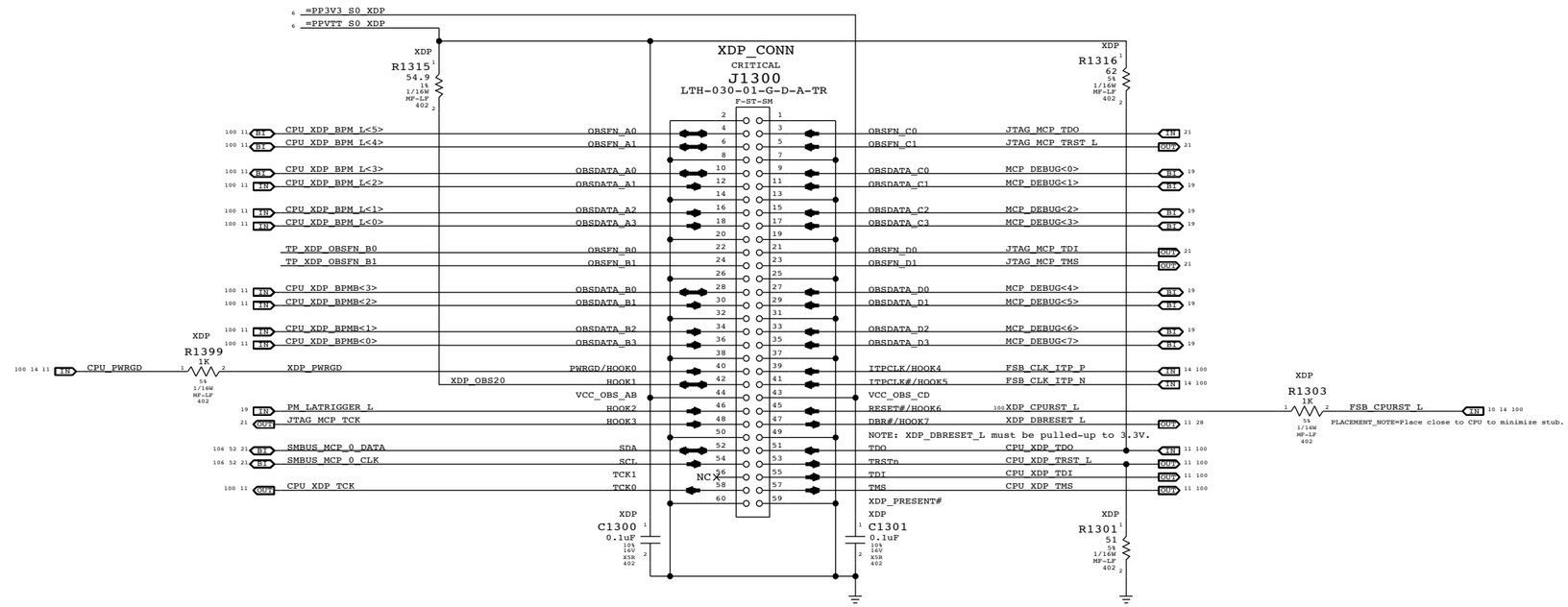
MCP79-specific pinout



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PAGE TITLE

eXtended Debug Port (XDP)

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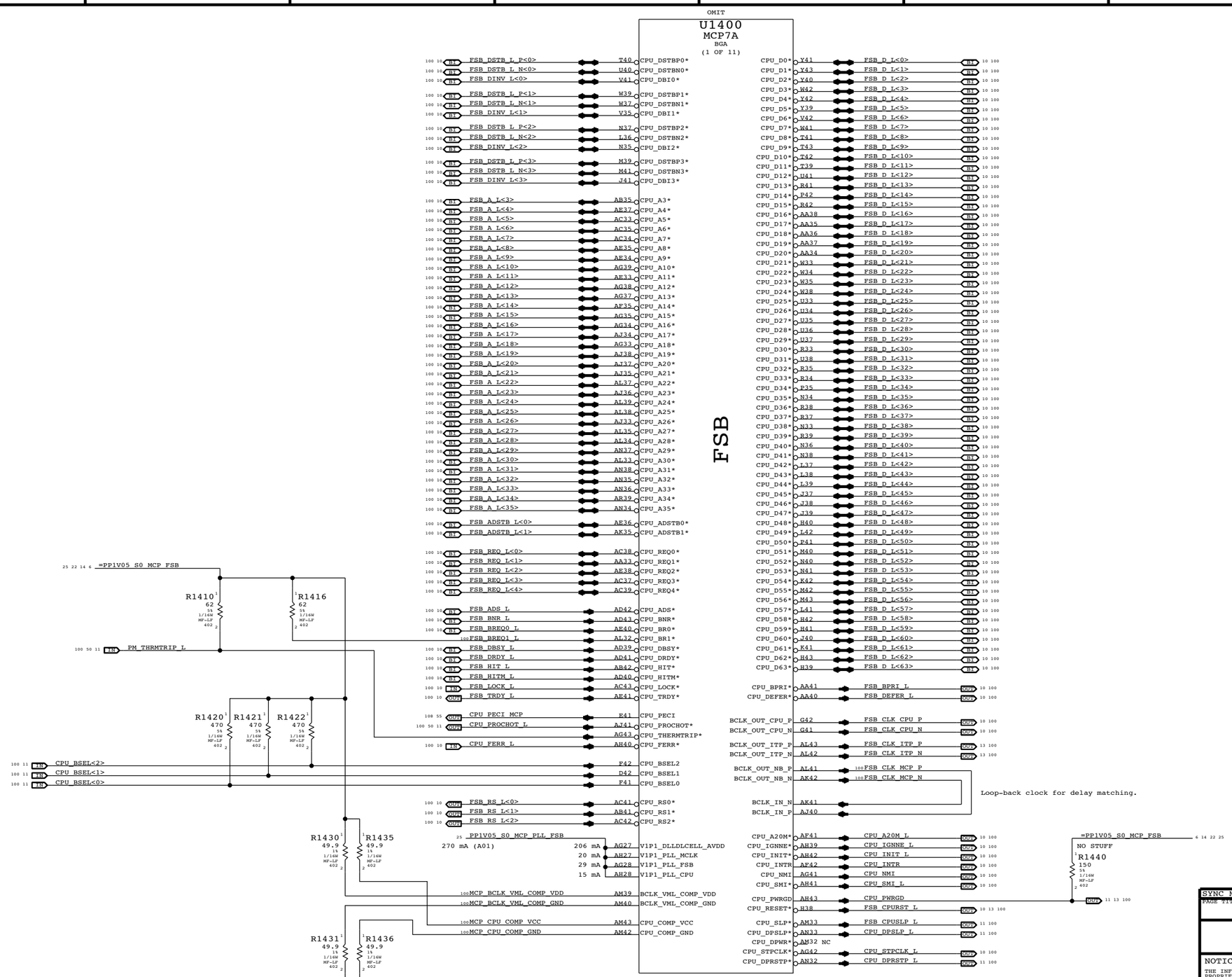

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SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

MCP CPU Interface

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

REVISION A.0.0

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PAGE 14 OF 110

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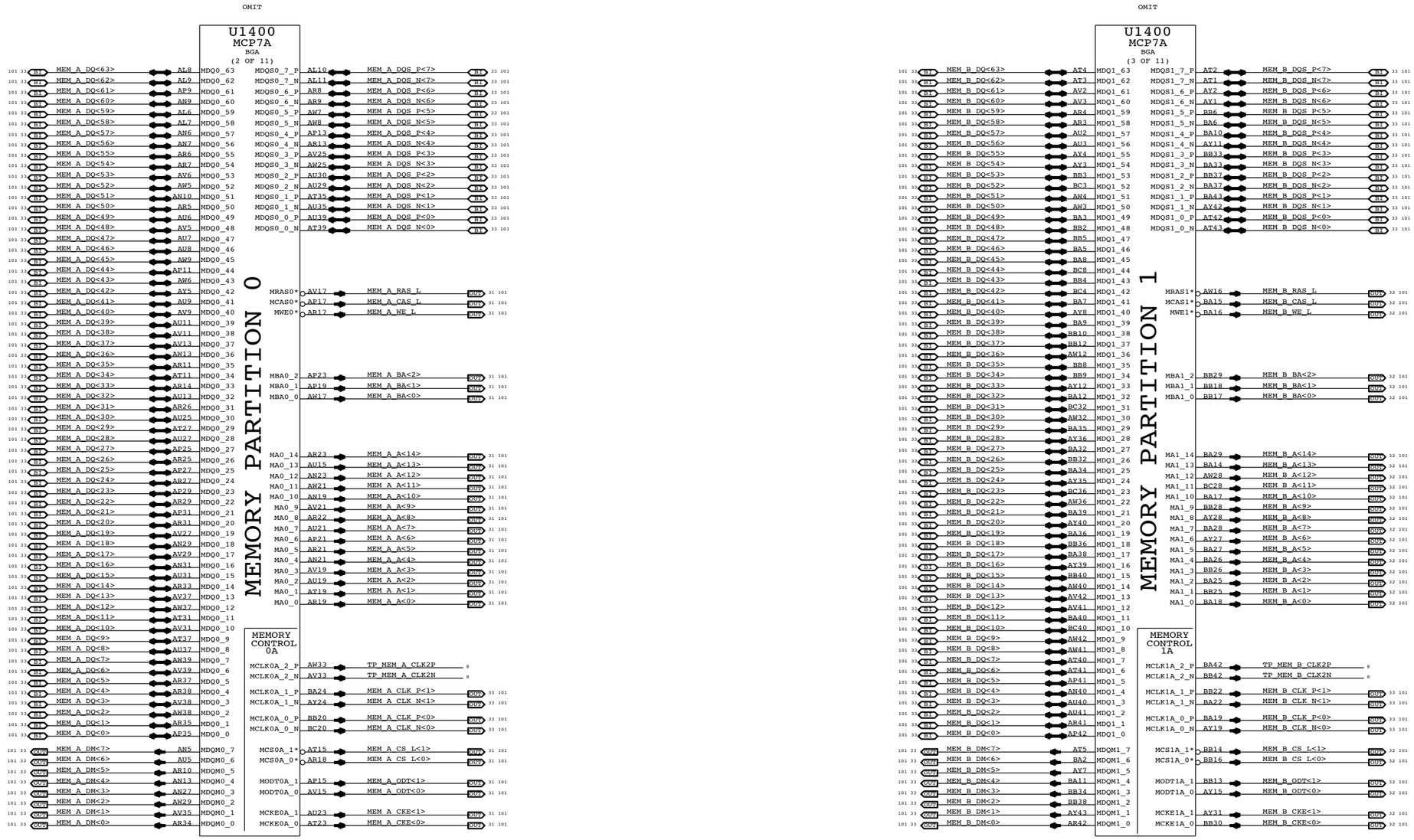

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

MCP Memory Interface

Apple Inc.

DRAWING NUMBER	051-7845
SIZE	D
REVISION	A.0.0
BRANCH	
PAGE	15 OF 110
SHEET	<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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OMIT

U1400 MCP7A
BGA
(4 OF 11)

MEMORY CONTROL 0B

8 TP_MEM_A_CLK5P	AU33	MCLK0B_2_P	
8 TP_MEM_A_CLK5N	AU34	MCLK0B_2_N	
101 33 MEM_A_CLK_P<4>	BB24	MCLK0B_1_P	
101 33 MEM_A_CLK_N<4>	BC24	MCLK0B_1_N	
101 33 MEM_A_CLK_P<3>	BA21	MCLK0B_0_P	
101 33 MEM_A_CLK_N<3>	BB21	MCLK0B_0_N	
101 31 MEM_A_CS_L<2>	AU17	MCS0B_0*	
101 31 MEM_A_CS_L<3>	AR15	MCS0B_1*	
101 31 MEM_A_ODT<2>	AN17	MODT0B_0	
101 31 MEM_A_ODT<3>	AN15	MODT0B_1	
101 31 MEM_A_CKE<2>	AV23	MCKE0B_0	
101 31 MEM_A_CKE<3>	AN25	MCKE0B_1	
25 PP1V05_S0_MCP_PLL_CORE 87 mA (A01)	17 mA T28	V1P1_PLL_V	
	12 mA U28	V1P1_PLL_DP	
	19 mA U27	V1P1_PLL_CORE	
	39 mA T27	V1P1_PLL_XREF_XS	
101 MCP_MEM_COMP_GND	AM41	MEM_COMP_GND	
101 MCP_MEM_COMP_VDD	AN41	MEM_COMP_1P8V	
	AA22	GND	
	AP12	GND	
	G30	GND	
	P10	GND	
	T10	GND	
	T6	GND	
	V10	GND	
	V34	GND	
	W5	GND	
	AA39	GND	
	AB22	GND	
	AB7	GND	
	AD22	GND	
	AE20	GND	
	AF24	GND	
	AG24	GND	
	AH35	GND	
	AK7	GND	
	AM28	GND	
	AT25	GND	
	AP30	GND	
	AR36	GND	
	AU10	GND	
	F28	GND	
	BC21	GND	
	AY9	GND	
	BC9	GND	
	D34	GND	
	F24	GND	
	G32	GND	
	H31	GND	
	K7	GND	
	M38	GND	
	M5	GND	
	M6	GND	
	M7	GND	
	M9	GND	
	N39	GND	
	N8	GND	
	P33	GND	
	P34	GND	
	P37	GND	
	P4	GND	
	P40	GND	
	P7	GND	
	R36	GND	
	R40	GND	
	R43	GND	
	R5	GND	
	T18	GND	
	T20	GND	
	AK11	GND	
	T24	GND	
	T26	GND	

MEMORY CONTROL 1B

	MCLK1B_2_P	BA41	TP_MEM_B_CLK5P 8
	MCLK1B_2_N	BB41	TP_MEM_B_CLK5N 8
	MCLK1B_1_P	AY23	MEM_B_CLK_P<4> 33 101
	MCLK1B_1_N	BA23	MEM_B_CLK_N<4> 33 101
	MCLK1B_0_P	BA20	MEM_B_CLK_P<3> 33 101
	MCLK1B_0_N	AY20	MEM_B_CLK_N<3> 33 101
	MCS1B_0*	BC16	MEM_B_CS_L<2> 32 101
	MCS1B_1*	BA13	MEM_B_CS_L<3> 32 101
	MODT1B_0	AY16	MEM_B_ODT<2> 32 101
	MODT1B_1	BC13	MEM_B_ODT<3> 32 101
	MCKE1B_0	BA30	MEM_B_CKE<2> 32 101
	MCKE1B_1	BA31	MEM_B_CKE<3> 32 101
	MRESET0*	AY32	MCP_MEM_RESET_L ODD 33
			TP or NC for DDR2.
		AM17	=PP1V8R1V5_S0_MCP_MEM 6 16 25 30
		AN20	4771 mA (A01, DDR3)
		AN24	V1P8_MEM_VDDP
		AT17	V1P8_MEM_VDDP
		AP16	V1P8_MEM_VDDP
		AN22	V1P8_MEM_VDDP
		AP20	V1P8_MEM_VDDP
		AP24	V1P8_MEM_VDDP
		AV16	V1P8_MEM_VDDP
		AR16	V1P8_MEM_VDDP
		AR20	V1P8_MEM_VDDP
		AM19	V1P8_MEM_VDDP
		AR24	V1P8_MEM_VDDP
		AW15	V1P8_MEM_VDDP
		AP22	V1P8_MEM_VDDP
		AP18	V1P8_MEM_VDDP
		AU16	V1P8_MEM_VDDP
		AN18	V1P8_MEM_VDDP
		AU24	V1P8_MEM_VDDP
		AT21	V1P8_MEM_VDDP
		AY29	V1P8_MEM_VDDP
		AV24	V1P8_MEM_VDDP
		AM21	V1P8_MEM_VDDP
		AU20	V1P8_MEM_VDDP
		AU22	V1P8_MEM_VDDP
		AW27	V1P8_MEM_VDDP
		BC17	V1P8_MEM_VDDP
		AV20	V1P8_MEM_VDDP
		AY17	V1P8_MEM_VDDP
		AY18	V1P8_MEM_VDDP
		AM15	V1P8_MEM_VDDP
		AU18	V1P8_MEM_VDDP
		AY25	V1P8_MEM_VDDP
		AM23	V1P8_MEM_VDDP
		AY26	V1P8_MEM_VDDP
		AW19	V1P8_MEM_VDDP
		AW24	V1P8_MEM_VDDP
		BC25	V1P8_MEM_VDDP
		AL30	V1P8_MEM_VDDP
		AM31	V1P8_MEM_VDDP
		AM25	V1P8_MEM_VDDP
		AM27	V1P8_MEM_VDDP
		AM29	V1P8_MEM_VDDP
		AN16	V1P8_MEM_VDDP
		BC29	V1P8_MEM_VDDP
		T33	GND
		T34	GND
		T35	GND
		T37	GND
		T38	GND
		T7	GND
		T9	GND
		U18	GND
		U20	GND
		U22	GND

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM

R1610[1] 40.2 1% 1/16W MF-LF 402 2

R1611[1] 40.2 1% 1/16W MF-LF 402 2

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SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
MCP MEMORY CNTRL & MISC

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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PAGE 16 OF 110

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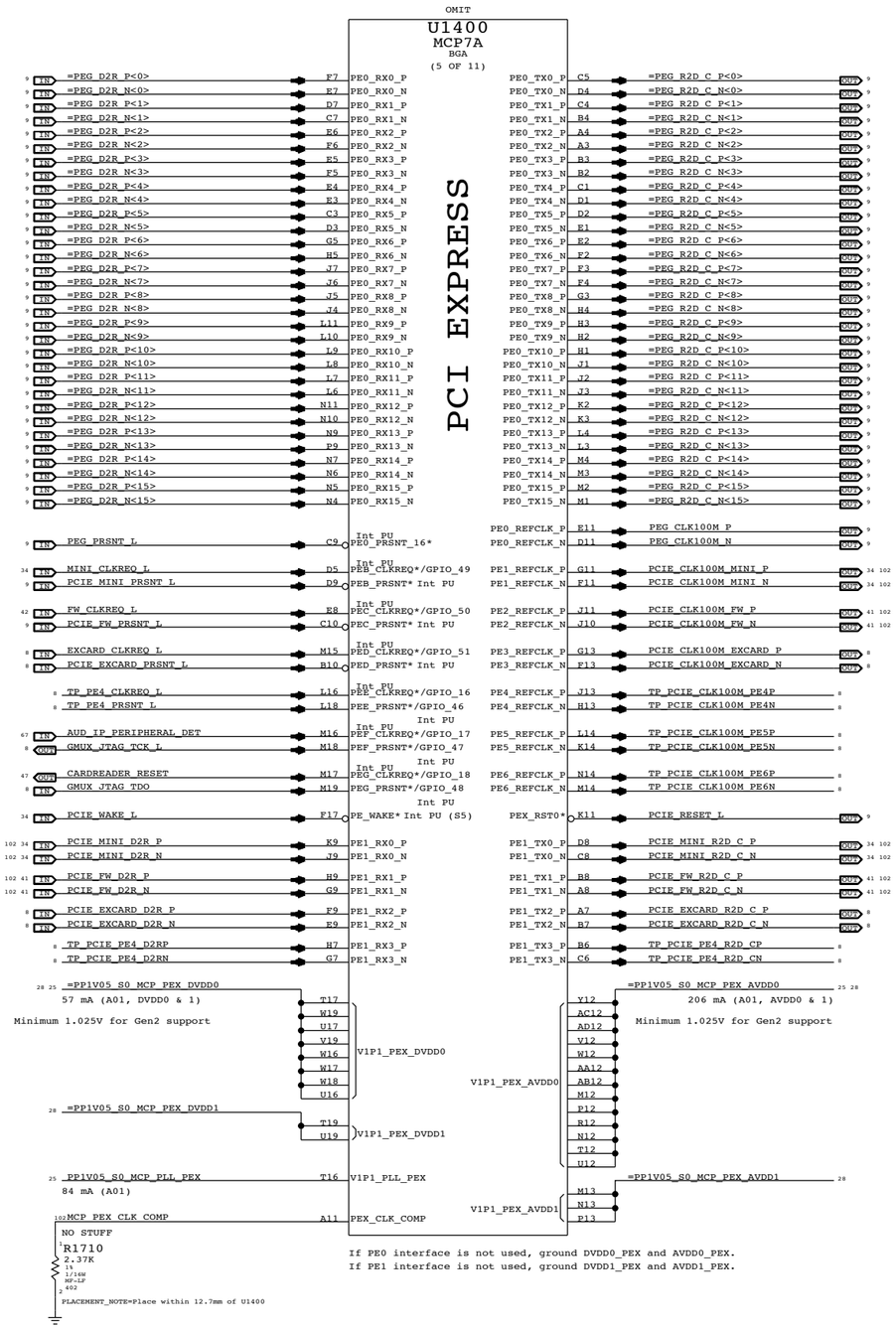

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PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

Interface Mode

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

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PAGE TITLE
MCP Ethernet & Graphics

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D
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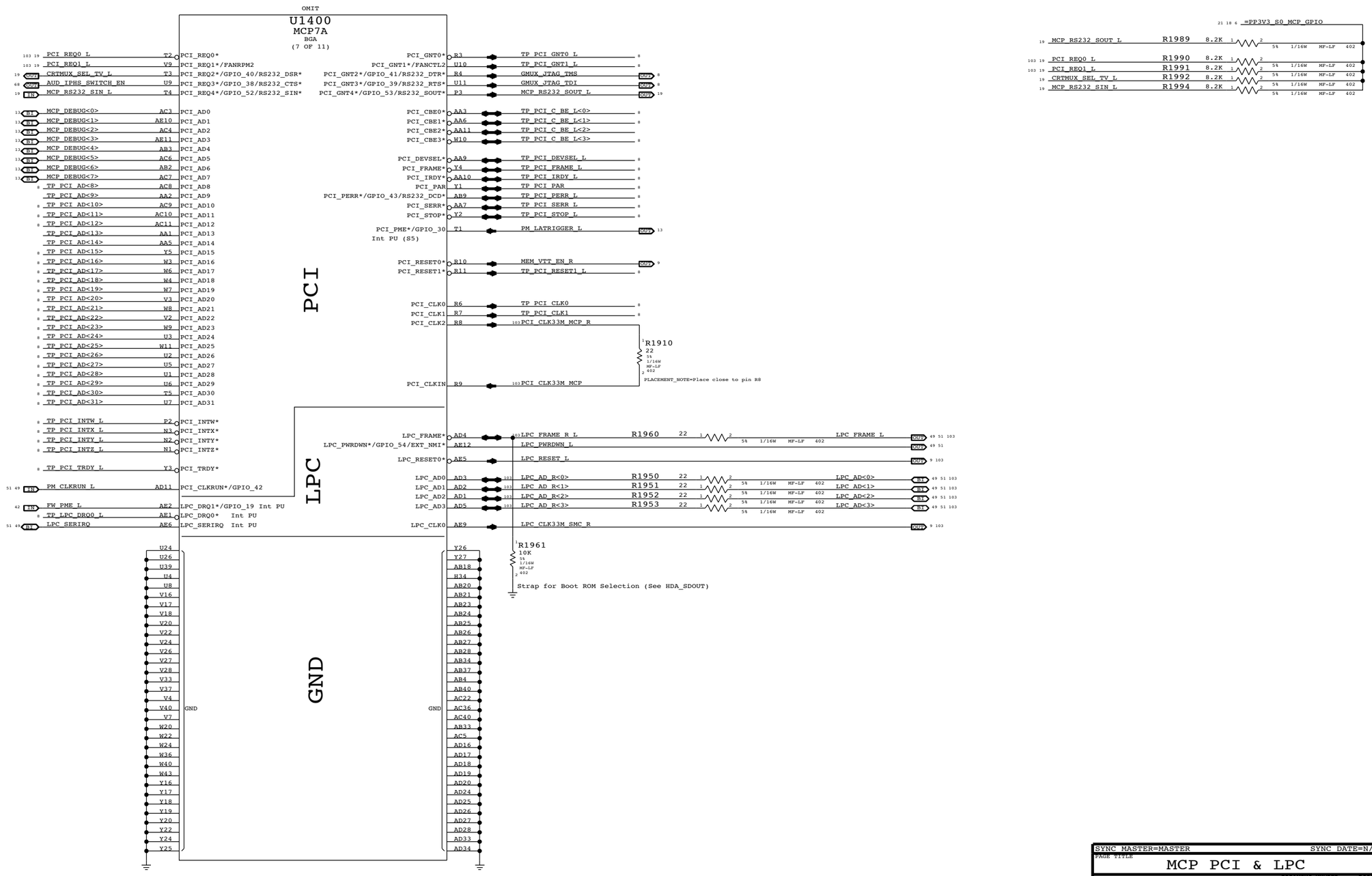

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PAGE TITLE

MCP PCI & LPC

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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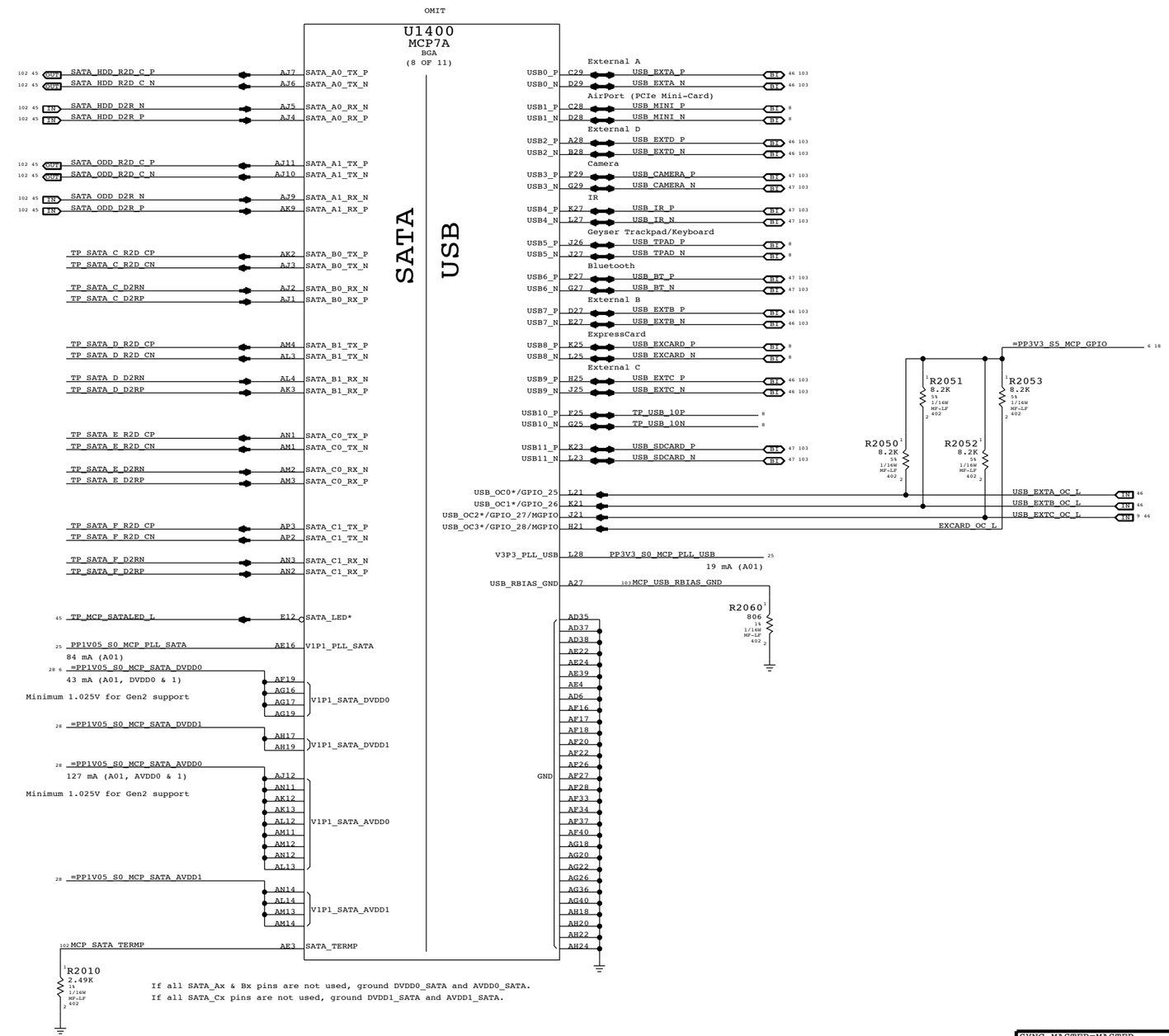

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PAGE TITLE
MCP SATA & USB

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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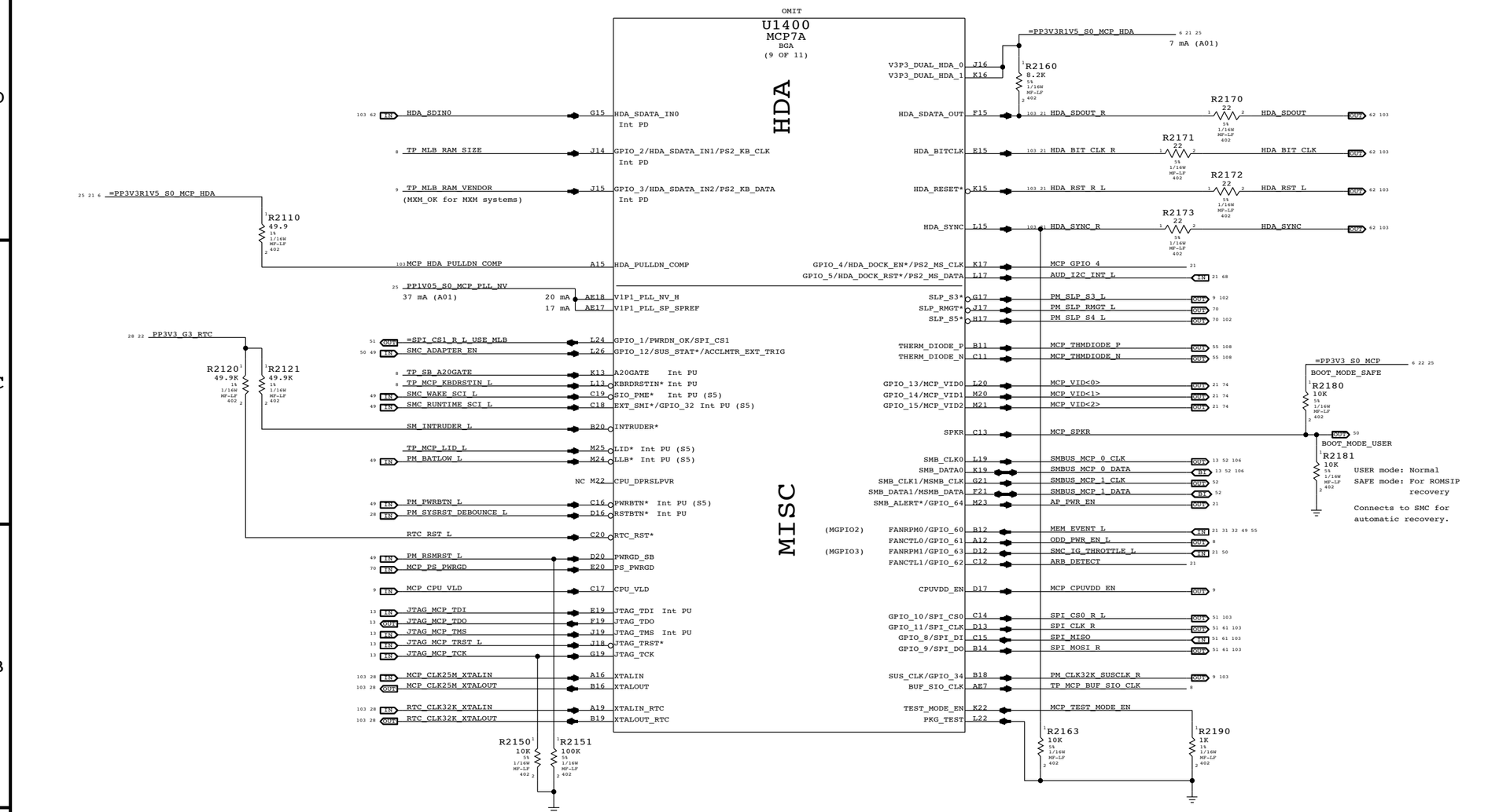


BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

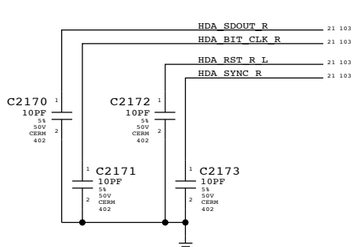
SPI Frequency Select

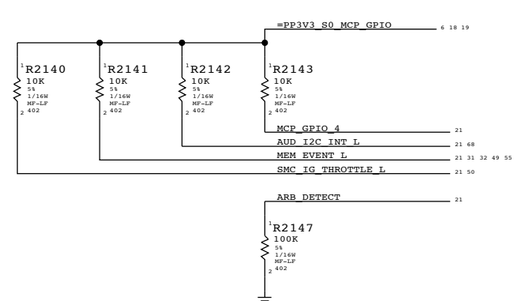
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

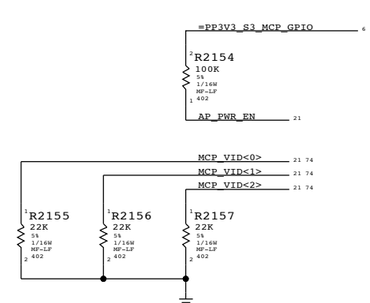
NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface







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PAGE TITLE: MCP HDA & MISC

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D

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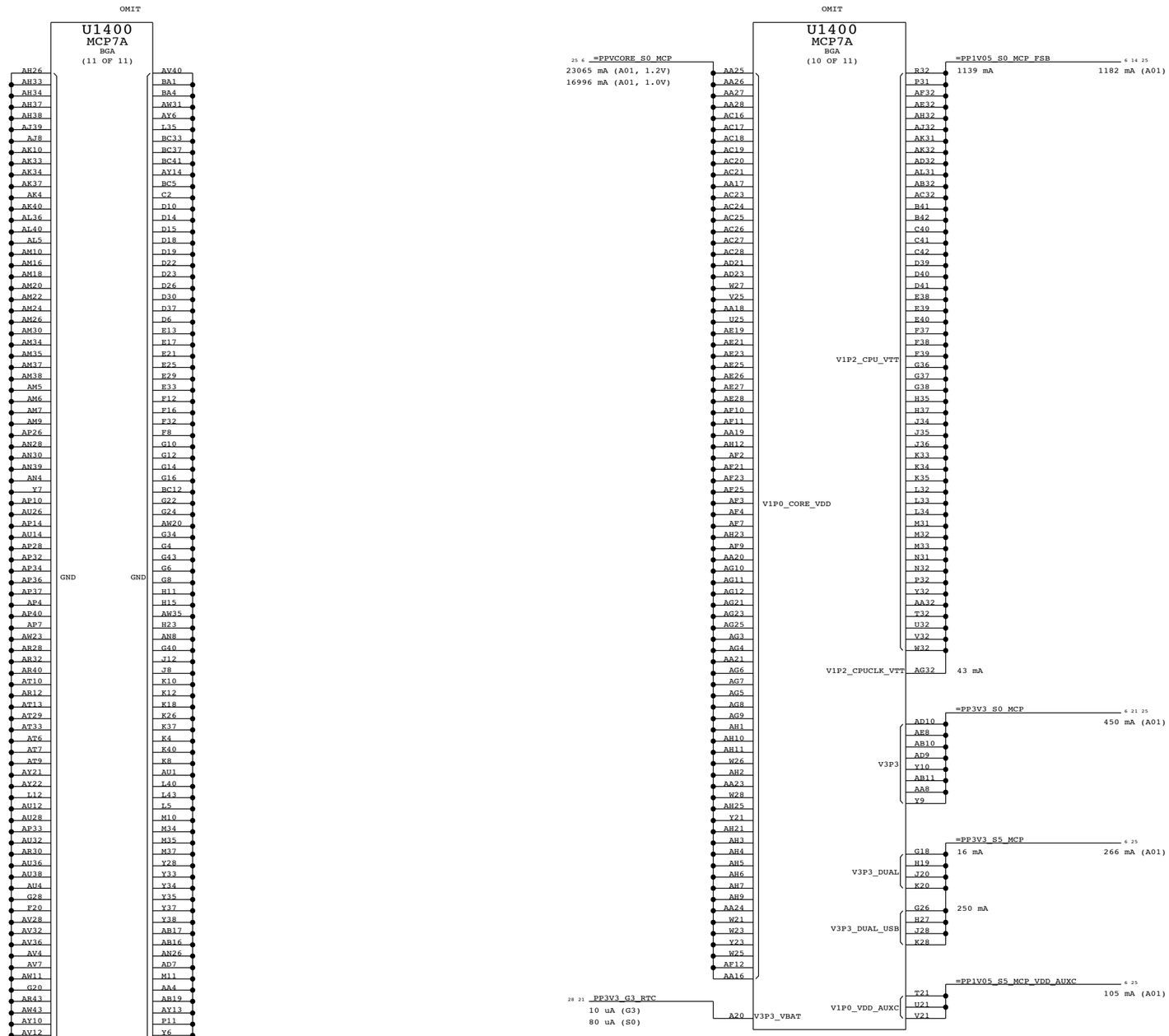

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PAGE TITLE
MCP Power & Ground

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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PAGE 23 OF 110

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Apple Inc.

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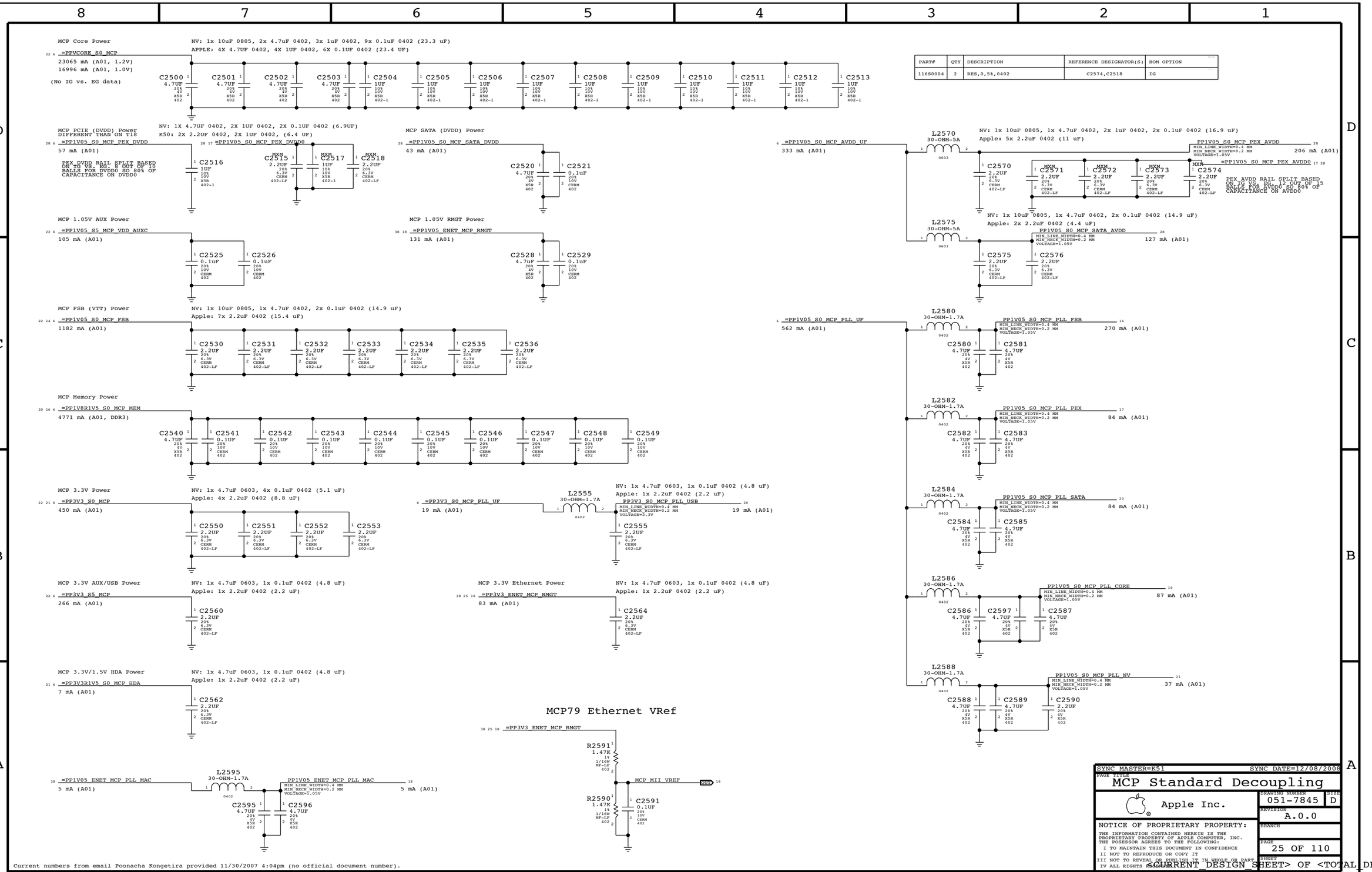
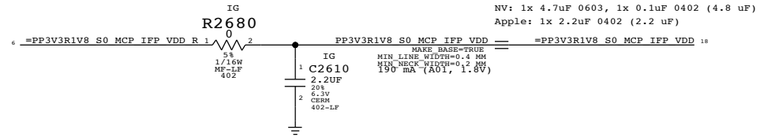


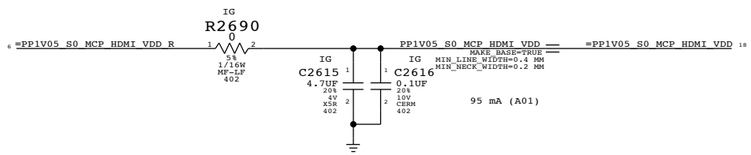
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	2	RES,0,5%,0402	C2574,C2518	IG

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

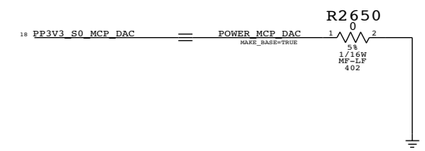
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

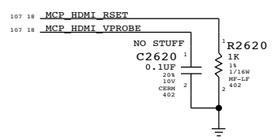


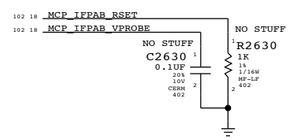
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2610		MXM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2616		MXM

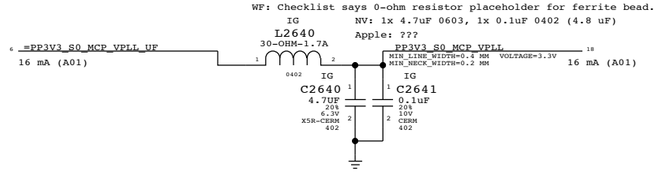






WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2641		MXM

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
MCP Graphics Support

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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PAGE TITLE

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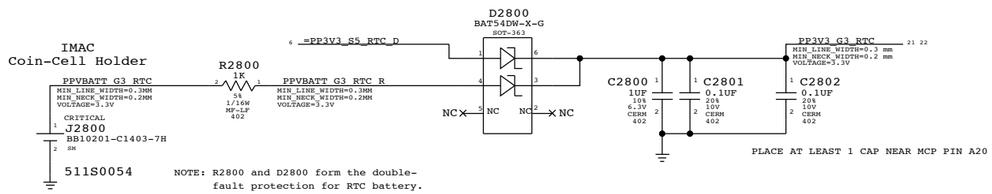
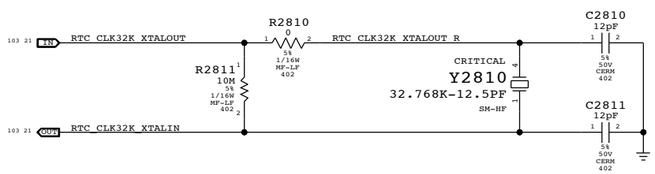
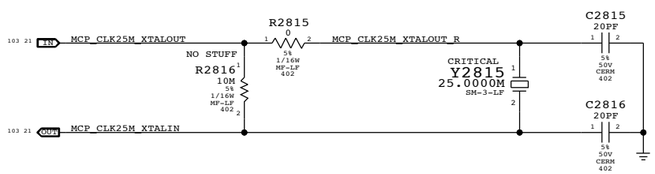
RTC Power Sources



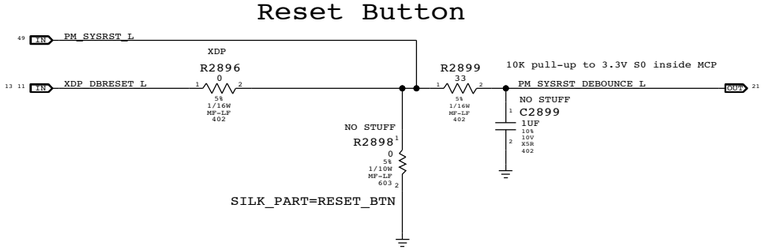
RTC Crystal



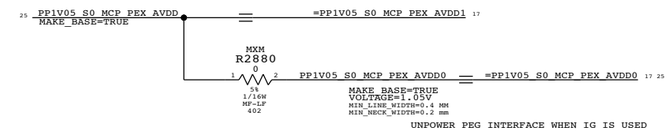
MCP 25MHz Crystal

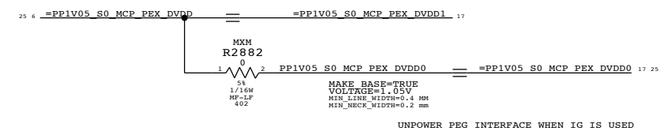


Reset Button

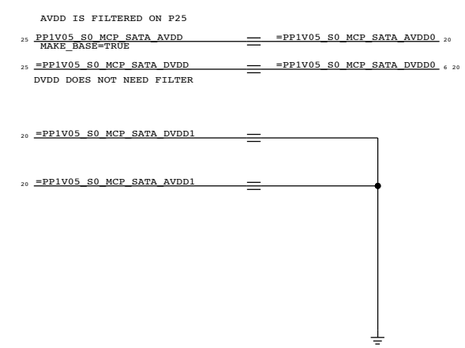


PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN





SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
SB Misc

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Page Notes

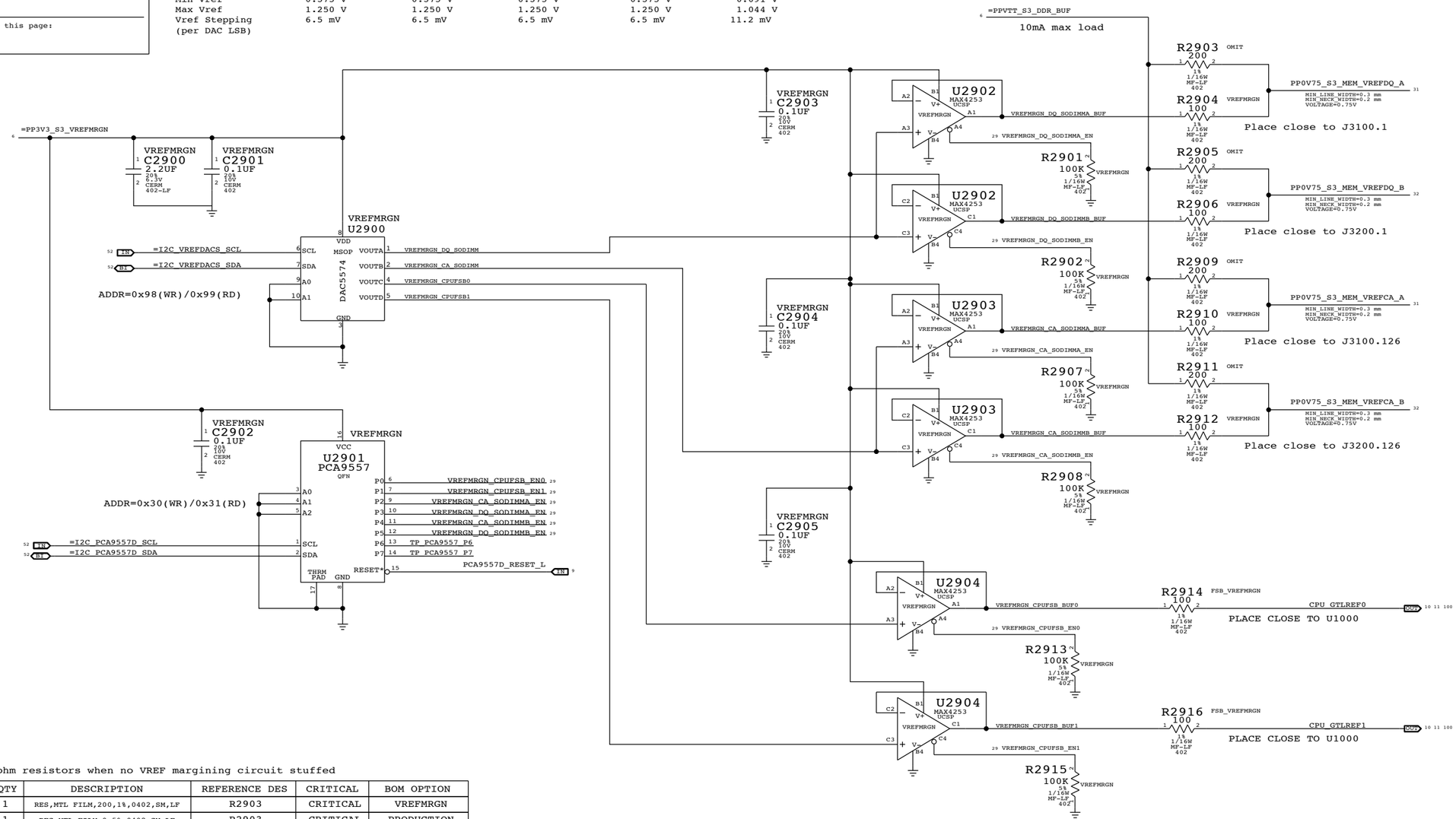
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
PRODUCTION

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2903	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2905	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2909	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2911	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	PRODUCTION

SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE
FSB/DDR3 Vref Margining

Apple Inc.

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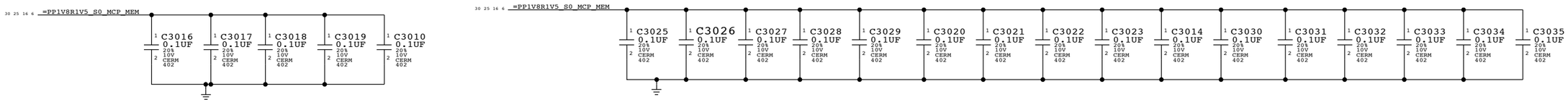
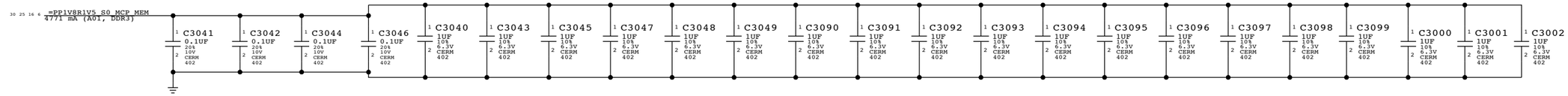
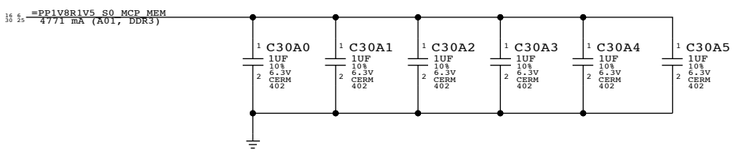
DIMM A (FURTHER FROM MCP) CAPS TO COUPLE MCP 1V5_S0_MEM DIMM B (CLOSER TO MCP)

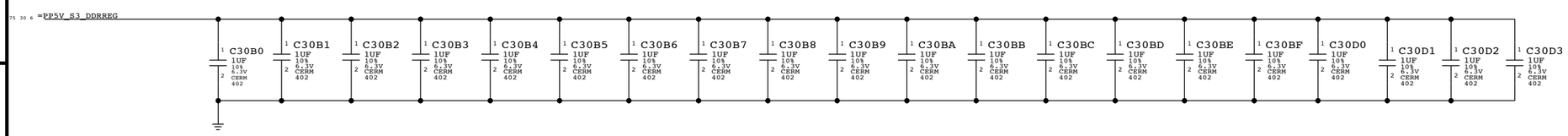


EXTRA DECOUPLING CAPS FOR MCP MEM RAIL

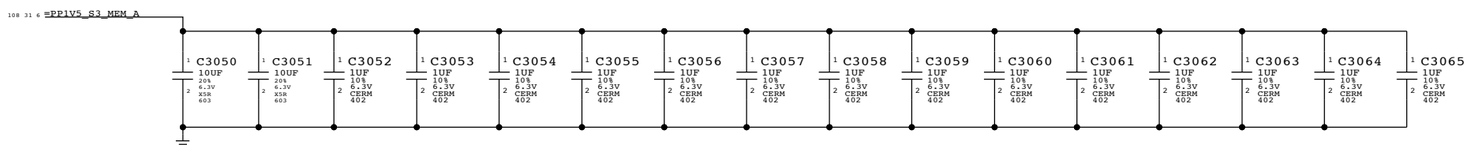




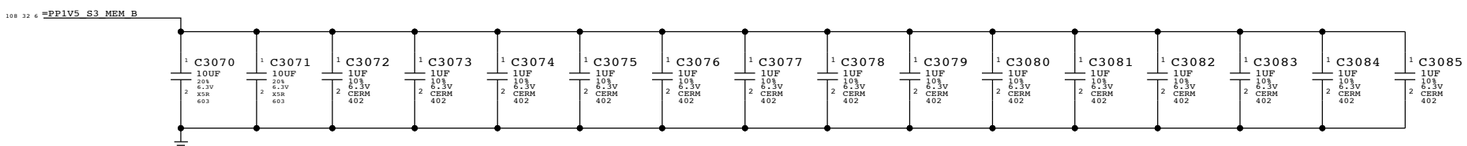
CAPS TO COUPLE PP5V_S3 UNDER DIMM CONNECTORS



DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR



DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

MEMORY CAPS

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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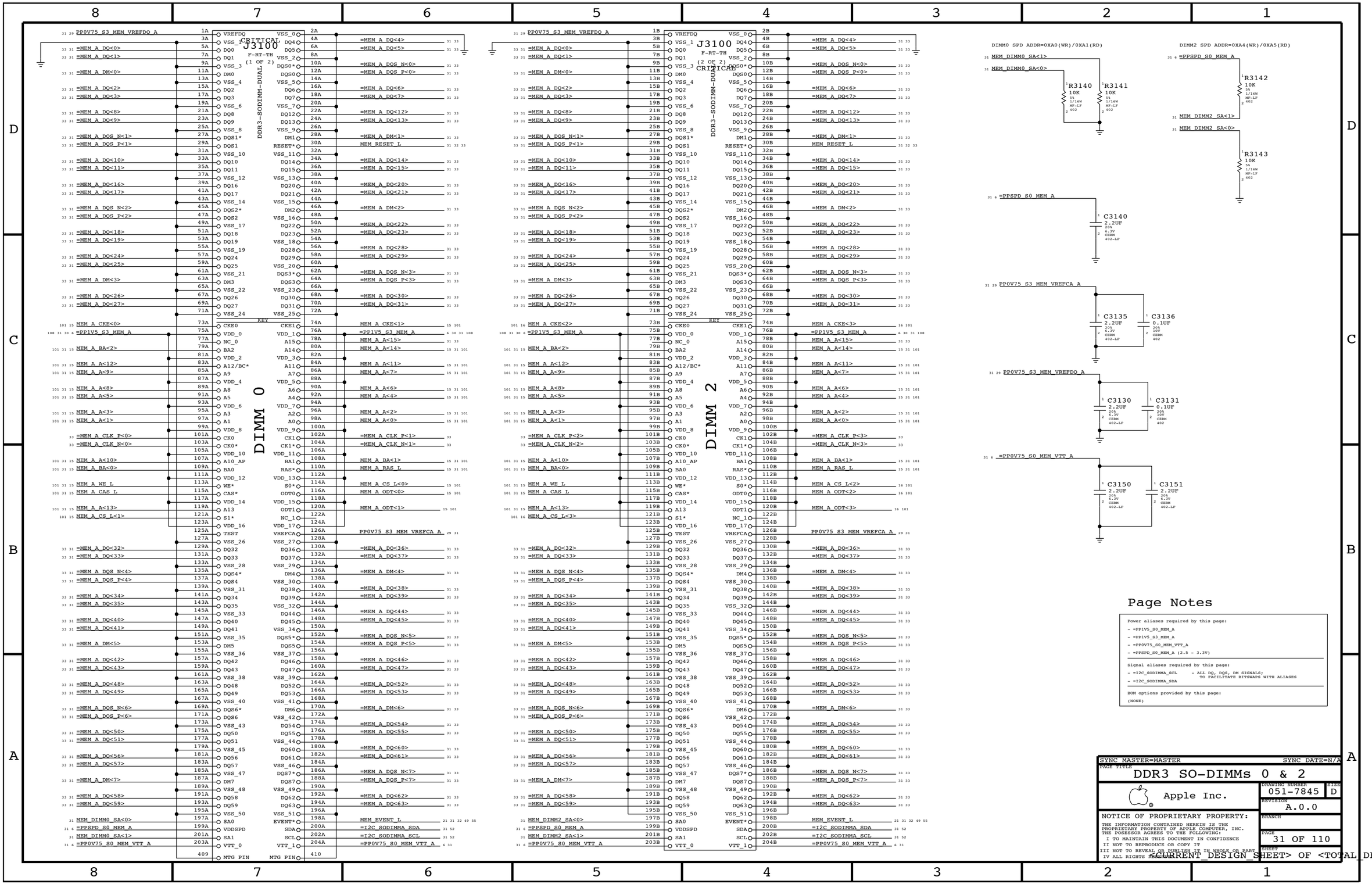

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL - ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: DDR3 SO-DIMMs 0 & 2

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

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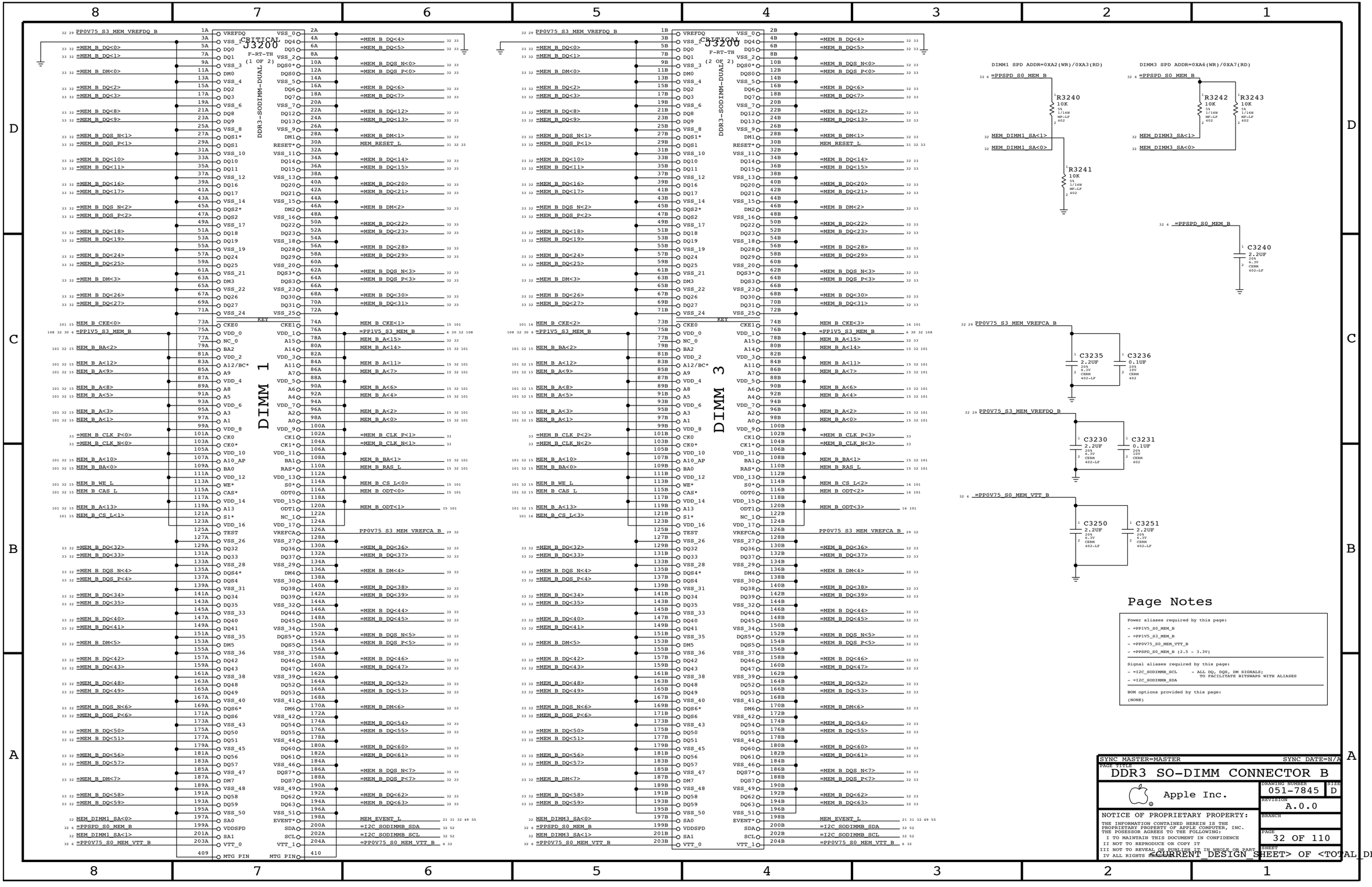

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL — ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)

SYNC MASTER=MASTER	SYNC DATE=N/A
PAGE TITLE: DDR3 SO-DIMM CONNECTOR B	
Apple Inc.	DRAWING NUMBER: 051-7845 SIZE: D
	REVISION: A.0.0
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	PAGE: 32 OF 110
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE		=MEM_A_DQS_N<0>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE		=MEM_A_DQS_P<0>
MEM_A_DM<0>	MAKE_BASE=TRUE		=MEM_A_DM<0>
MEM_A_DQ<7>	MAKE_BASE=TRUE		=MEM_A_DQ<7>
MEM_A_DQ<6>	MAKE_BASE=TRUE		=MEM_A_DQ<6>
MEM_A_DQ<5>	MAKE_BASE=TRUE		=MEM_A_DQ<4>
MEM_A_DQ<4>	MAKE_BASE=TRUE		=MEM_A_DQ<5>
MEM_A_DQ<3>	MAKE_BASE=TRUE		=MEM_A_DQ<3>
MEM_A_DQ<2>	MAKE_BASE=TRUE		=MEM_A_DQ<2>
MEM_A_DQ<1>	MAKE_BASE=TRUE		=MEM_A_DQ<0>
MEM_A_DQ<0>	MAKE_BASE=TRUE		=MEM_A_DQ<1>

MCP CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE		=MEM_A_DQS_N<1>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE		=MEM_A_DQS_P<1>
MEM_A_DM<1>	MAKE_BASE=TRUE		=MEM_A_DM<1>
MEM_A_DQ<15>	MAKE_BASE=TRUE		=MEM_A_DQ<15>
MEM_A_DQ<14>	MAKE_BASE=TRUE		=MEM_A_DQ<14>
MEM_A_DQ<13>	MAKE_BASE=TRUE		=MEM_A_DQ<13>
MEM_A_DQ<12>	MAKE_BASE=TRUE		=MEM_A_DQ<12>
MEM_A_DQ<11>	MAKE_BASE=TRUE		=MEM_A_DQ<11>
MEM_A_DQ<10>	MAKE_BASE=TRUE		=MEM_A_DQ<10>
MEM_A_DQ<9>	MAKE_BASE=TRUE		=MEM_A_DQ<8>
MEM_A_DQ<8>	MAKE_BASE=TRUE		=MEM_A_DQ<9>

MCP CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE		=MEM_A_DQS_N<2>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE		=MEM_A_DQS_P<2>
MEM_A_DM<2>	MAKE_BASE=TRUE		=MEM_A_DM<2>
MEM_A_DQ<23>	MAKE_BASE=TRUE		=MEM_A_DQ<23>
MEM_A_DQ<22>	MAKE_BASE=TRUE		=MEM_A_DQ<22>
MEM_A_DQ<21>	MAKE_BASE=TRUE		=MEM_A_DQ<16>
MEM_A_DQ<20>	MAKE_BASE=TRUE		=MEM_A_DQ<20>
MEM_A_DQ<19>	MAKE_BASE=TRUE		=MEM_A_DQ<19>
MEM_A_DQ<18>	MAKE_BASE=TRUE		=MEM_A_DQ<17>
MEM_A_DQ<17>	MAKE_BASE=TRUE		=MEM_A_DQ<18>
MEM_A_DQ<16>	MAKE_BASE=TRUE		=MEM_A_DQ<21>

MCP CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE		=MEM_A_DQS_N<3>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE		=MEM_A_DQS_P<3>
MEM_A_DM<3>	MAKE_BASE=TRUE		=MEM_A_DM<3>
MEM_A_DQ<31>	MAKE_BASE=TRUE		=MEM_A_DQ<31>
MEM_A_DQ<30>	MAKE_BASE=TRUE		=MEM_A_DQ<30>
MEM_A_DQ<29>	MAKE_BASE=TRUE		=MEM_A_DQ<29>
MEM_A_DQ<28>	MAKE_BASE=TRUE		=MEM_A_DQ<28>
MEM_A_DQ<27>	MAKE_BASE=TRUE		=MEM_A_DQ<27>
MEM_A_DQ<26>	MAKE_BASE=TRUE		=MEM_A_DQ<26>
MEM_A_DQ<25>	MAKE_BASE=TRUE		=MEM_A_DQ<25>
MEM_A_DQ<24>	MAKE_BASE=TRUE		=MEM_A_DQ<24>

MCP CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE		=MEM_A_DQS_N<4>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE		=MEM_A_DQS_P<4>
MEM_A_DM<4>	MAKE_BASE=TRUE		=MEM_A_DM<4>
MEM_A_DQ<39>	MAKE_BASE=TRUE		=MEM_A_DQ<39>
MEM_A_DQ<38>	MAKE_BASE=TRUE		=MEM_A_DQ<38>
MEM_A_DQ<37>	MAKE_BASE=TRUE		=MEM_A_DQ<37>
MEM_A_DQ<36>	MAKE_BASE=TRUE		=MEM_A_DQ<36>
MEM_A_DQ<35>	MAKE_BASE=TRUE		=MEM_A_DQ<35>
MEM_A_DQ<34>	MAKE_BASE=TRUE		=MEM_A_DQ<34>
MEM_A_DQ<33>	MAKE_BASE=TRUE		=MEM_A_DQ<33>
MEM_A_DQ<32>	MAKE_BASE=TRUE		=MEM_A_DQ<32>

MCP CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE		=MEM_A_DQS_N<5>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE		=MEM_A_DQS_P<5>
MEM_A_DM<5>	MAKE_BASE=TRUE		=MEM_A_DM<5>
MEM_A_DQ<47>	MAKE_BASE=TRUE		=MEM_A_DQ<47>
MEM_A_DQ<46>	MAKE_BASE=TRUE		=MEM_A_DQ<46>
MEM_A_DQ<45>	MAKE_BASE=TRUE		=MEM_A_DQ<45>
MEM_A_DQ<44>	MAKE_BASE=TRUE		=MEM_A_DQ<44>
MEM_A_DQ<43>	MAKE_BASE=TRUE		=MEM_A_DQ<43>
MEM_A_DQ<42>	MAKE_BASE=TRUE		=MEM_A_DQ<42>
MEM_A_DQ<41>	MAKE_BASE=TRUE		=MEM_A_DQ<41>
MEM_A_DQ<40>	MAKE_BASE=TRUE		=MEM_A_DQ<40>

MCP CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE		=MEM_A_DQS_N<6>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE		=MEM_A_DQS_P<6>
MEM_A_DM<6>	MAKE_BASE=TRUE		=MEM_A_DM<6>
MEM_A_DQ<55>	MAKE_BASE=TRUE		=MEM_A_DQ<55>
MEM_A_DQ<54>	MAKE_BASE=TRUE		=MEM_A_DQ<54>
MEM_A_DQ<53>	MAKE_BASE=TRUE		=MEM_A_DQ<53>
MEM_A_DQ<52>	MAKE_BASE=TRUE		=MEM_A_DQ<52>
MEM_A_DQ<51>	MAKE_BASE=TRUE		=MEM_A_DQ<51>
MEM_A_DQ<50>	MAKE_BASE=TRUE		=MEM_A_DQ<50>
MEM_A_DQ<49>	MAKE_BASE=TRUE		=MEM_A_DQ<49>
MEM_A_DQ<48>	MAKE_BASE=TRUE		=MEM_A_DQ<48>

MCP CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE		=MEM_A_DQS_N<7>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE		=MEM_A_DQS_P<7>
MEM_A_DM<7>	MAKE_BASE=TRUE		=MEM_A_DM<7>
MEM_A_DQ<63>	MAKE_BASE=TRUE		=MEM_A_DQ<63>
MEM_A_DQ<62>	MAKE_BASE=TRUE		=MEM_A_DQ<62>
MEM_A_DQ<61>	MAKE_BASE=TRUE		=MEM_A_DQ<57>
MEM_A_DQ<60>	MAKE_BASE=TRUE		=MEM_A_DQ<56>
MEM_A_DQ<59>	MAKE_BASE=TRUE		=MEM_A_DQ<59>
MEM_A_DQ<58>	MAKE_BASE=TRUE		=MEM_A_DQ<58>
MEM_A_DQ<57>	MAKE_BASE=TRUE		=MEM_A_DQ<61>
MEM_A_DQ<56>	MAKE_BASE=TRUE		=MEM_A_DQ<60>

MCP CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQS_N<0>	MAKE_BASE=TRUE		=MEM_B_DQS_N<0>
MEM_B_DQS_P<0>	MAKE_BASE=TRUE		=MEM_B_DQS_P<0>
MEM_B_DM<0>	MAKE_BASE=TRUE		=MEM_B_DM<0>
MEM_B_DQ<7>	MAKE_BASE=TRUE		=MEM_B_DQ<7>
MEM_B_DQ<6>	MAKE_BASE=TRUE		=MEM_B_DQ<6>
MEM_B_DQ<5>	MAKE_BASE=TRUE		=MEM_B_DQ<1>
MEM_B_DQ<4>	MAKE_BASE=TRUE		=MEM_B_DQ<0>
MEM_B_DQ<3>	MAKE_BASE=TRUE		=MEM_B_DQ<3>
MEM_B_DQ<2>	MAKE_BASE=TRUE		=MEM_B_DQ<2>
MEM_B_DQ<1>	MAKE_BASE=TRUE		=MEM_B_DQ<5>
MEM_B_DQ<0>	MAKE_BASE=TRUE		=MEM_B_DQ<4>

MCP CHANNEL B DQS 1 -> DIMM B DQS 1

MEM_B_DQS_N<1>	MAKE_BASE=TRUE		=MEM_B_DQS_N<1>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE		=MEM_B_DQS_P<1>
MEM_B_DM<1>	MAKE_BASE=TRUE		=MEM_B_DM<1>
MEM_B_DQ<15>	MAKE_BASE=TRUE		=MEM_B_DQ<15>
MEM_B_DQ<14>	MAKE_BASE=TRUE		=MEM_B_DQ<14>
MEM_B_DQ<13>	MAKE_BASE=TRUE		=MEM_B_DQ<13>
MEM_B_DQ<12>	MAKE_BASE=TRUE		=MEM_B_DQ<12>
MEM_B_DQ<11>	MAKE_BASE=TRUE		=MEM_B_DQ<11>
MEM_B_DQ<10>	MAKE_BASE=TRUE		=MEM_B_DQ<10>
MEM_B_DQ<9>	MAKE_BASE=TRUE		=MEM_B_DQ<9>
MEM_B_DQ<8>	MAKE_BASE=TRUE		=MEM_B_DQ<8>

MCP CHANNEL B DQS 2 -> DIMM B DQS 2

MEM_B_DQS_N<2>	MAKE_BASE=TRUE		=MEM_B_DQS_N<2>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE		=MEM_B_DQS_P<2>
MEM_B_DM<2>	MAKE_BASE=TRUE		=MEM_B_DM<2>
MEM_B_DQ<23>	MAKE_BASE=TRUE		=MEM_B_DQ<23>
MEM_B_DQ<22>	MAKE_BASE=TRUE		=MEM_B_DQ<22>
MEM_B_DQ<21>	MAKE_BASE=TRUE		=MEM_B_DQ<21>
MEM_B_DQ<20>	MAKE_BASE=TRUE		=MEM_B_DQ<20>
MEM_B_DQ<19>	MAKE_BASE=TRUE		=MEM_B_DQ<19>
MEM_B_DQ<18>	MAKE_BASE=TRUE		=MEM_B_DQ<18>
MEM_B_DQ<17>	MAKE_BASE=TRUE		=MEM_B_DQ<17>
MEM_B_DQ<16>	MAKE_BASE=TRUE		=MEM_B_DQ<16>

MCP CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQS_N<3>	MAKE_BASE=TRUE		=MEM_B_DQS_N<3>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE		=MEM_B_DQS_P<3>
MEM_B_DM<3>	MAKE_BASE=TRUE		=MEM_B_DM<3>
MEM_B_DQ<31>	MAKE_BASE=TRUE		=MEM_B_DQ<31>
MEM_B_DQ<30>	MAKE_BASE=TRUE		=MEM_B_DQ<30>
MEM_B_DQ<29>	MAKE_BASE=TRUE		=MEM_B_DQ<29>
MEM_B_DQ<28>	MAKE_BASE=TRUE		=MEM_B_DQ<28>
MEM_B_DQ<27>	MAKE_BASE=TRUE		=MEM_B_DQ<27>
MEM_B_DQ<26>	MAKE_BASE=TRUE		=MEM_B_DQ<26>
MEM_B_DQ<25>	MAKE_BASE=TRUE		=MEM_B_DQ<25>
MEM_B_DQ<24>	MAKE_BASE=TRUE		=MEM_B_DQ<24>

MCP CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQS_N<4>	MAKE_BASE=TRUE		=MEM_B_DQS_N<4>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE		=MEM_B_DQS_P<4>
MEM_B_DM<4>	MAKE_BASE=TRUE		=MEM_B_DM<4>
MEM_B_DQ<39>	MAKE_BASE=TRUE		=MEM_B_DQ<39>
MEM_B_DQ<38>	MAKE_BASE=TRUE		=MEM_B_DQ<38>
MEM_B_DQ<37>	MAKE_BASE=TRUE		=MEM_B_DQ<37>
MEM_B_DQ<36>	MAKE_BASE=TRUE		=MEM_B_DQ<36>
MEM_B_DQ<35>	MAKE_BASE=TRUE		=MEM_B_DQ<35>
MEM_B_DQ<34>	MAKE_BASE=TRUE		=MEM_B_DQ<34>
MEM_B_DQ<33>	MAKE_BASE=TRUE		=MEM_B_DQ<33>
MEM_B_DQ<32>	MAKE_BASE=TRUE		=MEM_B_DQ<32>

MCP CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQS_N<5>	MAKE_BASE=TRUE		=MEM_B_DQS_N<5>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE		=MEM_B_DQS_P<5>
MEM_B_DM<5>	MAKE_BASE=TRUE		=MEM_B_DM<5>
MEM_B_DQ<47>	MAKE_BASE=TRUE		=MEM_B_DQ<47>
MEM_B_DQ<46>	MAKE_BASE=TRUE		=MEM_B_DQ<46>
MEM_B_DQ<45>	MAKE_BASE=TRUE		=MEM_B_DQ<45>
MEM_B_DQ<44>	MAKE_BASE=TRUE		=MEM_B_DQ<44>
MEM_B_DQ<43>	MAKE_BASE=TRUE		=MEM_B_DQ<43>
MEM_B_DQ<42>	MAKE_BASE=TRUE		=MEM_B_DQ<42>
MEM_B_DQ<41>	MAKE_BASE=TRUE		=MEM_B_DQ<41>
MEM_B_DQ<40>	MAKE_BASE=TRUE		=MEM_B_DQ<40>

MCP CHANNEL B DQS 6 -> DIMM B DQS 6

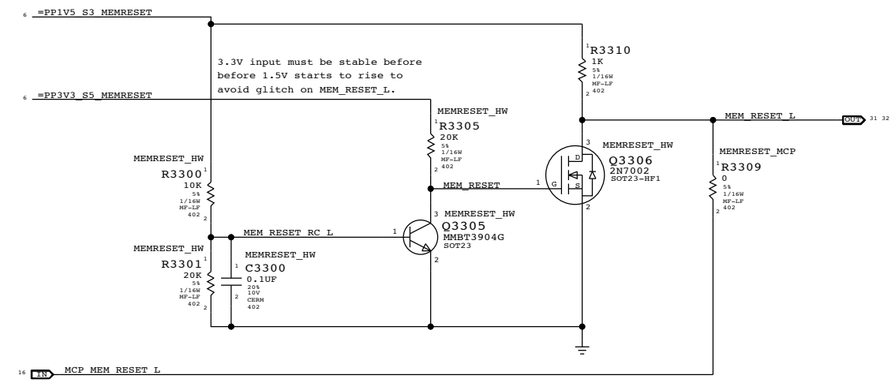
MEM_B_DQS_N<6>	MAKE_BASE=TRUE		=MEM_B_DQS_N<6>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE		=MEM_B_DQS_P<6>
MEM_B_DM<6>	MAKE_BASE=TRUE		=MEM_B_DM<6>
MEM_B_DQ<55>	MAKE_BASE=TRUE		=MEM_B_DQ<55>
MEM_B_DQ<54>	MAKE_BASE=TRUE		=MEM_B_DQ<54>
MEM_B_DQ<53>	MAKE_BASE=TRUE		=MEM_B_DQ<53>
MEM_B_DQ<52>	MAKE_BASE=TRUE		=MEM_B_DQ<52>
MEM_B_DQ<51>	MAKE_BASE=TRUE		=MEM_B_DQ<51>
MEM_B_DQ<50>	MAKE_BASE=TRUE		=MEM_B_DQ<50>
MEM_B_DQ<49>	MAKE_BASE=TRUE		
MEM_B_DQ<48>	MAKE_BASE=TRUE		=MEM_B_DQ<48>

MCP CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQS_N<7>	MAKE_BASE=TRUE		=MEM_B_DQS_N<7>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE		=MEM_B_DQS_P<7>
MEM_B_DM<7>	MAKE_BASE=TRUE		=MEM_B_DM<7>
MEM_B_DQ<63>	MAKE_BASE=TRUE		=MEM_B_DQ<63>
MEM_B_DQ<62>	MAKE_BASE=TRUE		=MEM_B_DQ<62>
MEM_B_DQ<61>	MAKE_BASE=TRUE		=MEM_B_DQ<61>
MEM_B_DQ<60>	MAKE_BASE=TRUE		=MEM_B_DQ<60>
MEM_B_DQ<59>	MAKE_BASE=TRUE		=MEM_B_DQ<59>
MEM_B_DQ<58>	MAKE_BASE=TRUE		=MEM_B_DQ<58>
MEM_B_DQ<57>	MAKE_BASE=TRUE		=MEM_B_DQ<57>
MEM_B_DQ<56>	MAKE_BASE=TRUE		=MEM_B_DQ<56>

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



MCP MEMORY CLOCK ALIASES

MEM_A_CLK_P<0>	MAKE_BASE=TRUE		=MEM_A_CLK_P<0>
MEM_A_CLK_N<0>	MAKE_BASE=TRUE		=MEM_A_CLK_N<0>
MEM_A_CLK_P<1>	MAKE_BASE=TRUE		=MEM_A_CLK_P<1>
MEM_A_CLK_N<1>	MAKE_BASE=TRUE		=MEM_A_CLK_N<1>
MEM_A_CLK_P<3>	MAKE_BASE=TRUE		=MEM_A_CLK_P<2>
MEM_A_CLK_N<3>	MAKE_BASE=TRUE		=MEM_A_CLK_N<2>
MEM_A_CLK_P<4>	MAKE_BASE=TRUE		=MEM_A_CLK_P<3>
MEM_A_CLK_N<4>	MAKE_BASE=TRUE		=MEM_A_CLK_N<3>
	MAKE_BASE=TRUE		

MEM_B_CLK_P<0>	MAKE_BASE=TRUE		=MEM_B_CLK_P<0>
MEM_B_CLK_N<0>	MAKE_BASE=TRUE		=MEM_B_CLK_N<0>
MEM_B_CLK_P<1>	MAKE_BASE=TRUE		=MEM_B_CLK_P<1>
MEM_B_CLK_N<1>	MAKE_BASE=TRUE		=MEM_B_CLK_N<1>
MEM_B_CLK_P<3>	MAKE_BASE=TRUE		=MEM_B_CLK_P<2>
MEM_B_CLK_N<3>	MAKE_BASE=TRUE		=MEM_B_CLK_N<2>
MEM_B_CLK_P<4>	MAKE_BASE=TRUE		=MEM_B_CLK_P<3>
MEM_B_CLK_N<4>	MAKE_BASE=TRUE		=MEM_B_CLK_N<3>
	MAKE_BASE=TRUE		

MCP MEMORY TEST POINT ALIASES

TP_MEM_A_A<15>			MEM_A_A<15>
TP_MEM_B_A<15>	MAKE_BASE=TRUE		MEM_B_A<15>
	MAKE_BASE=TRUE		

SYNC MASTER=K51 SYNC DATE=10/13/2008

PAGE TITLE
DDR3 SUPPORT AND BITSWAPS

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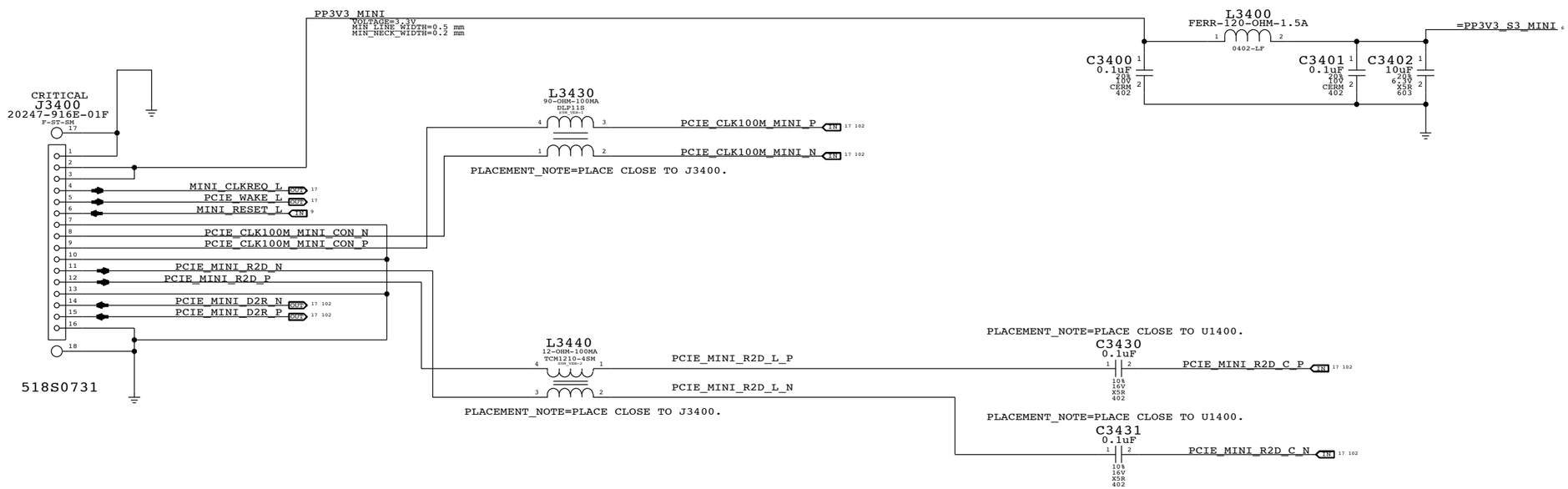

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PAGE TITLE

PCI-E Wireless Connector

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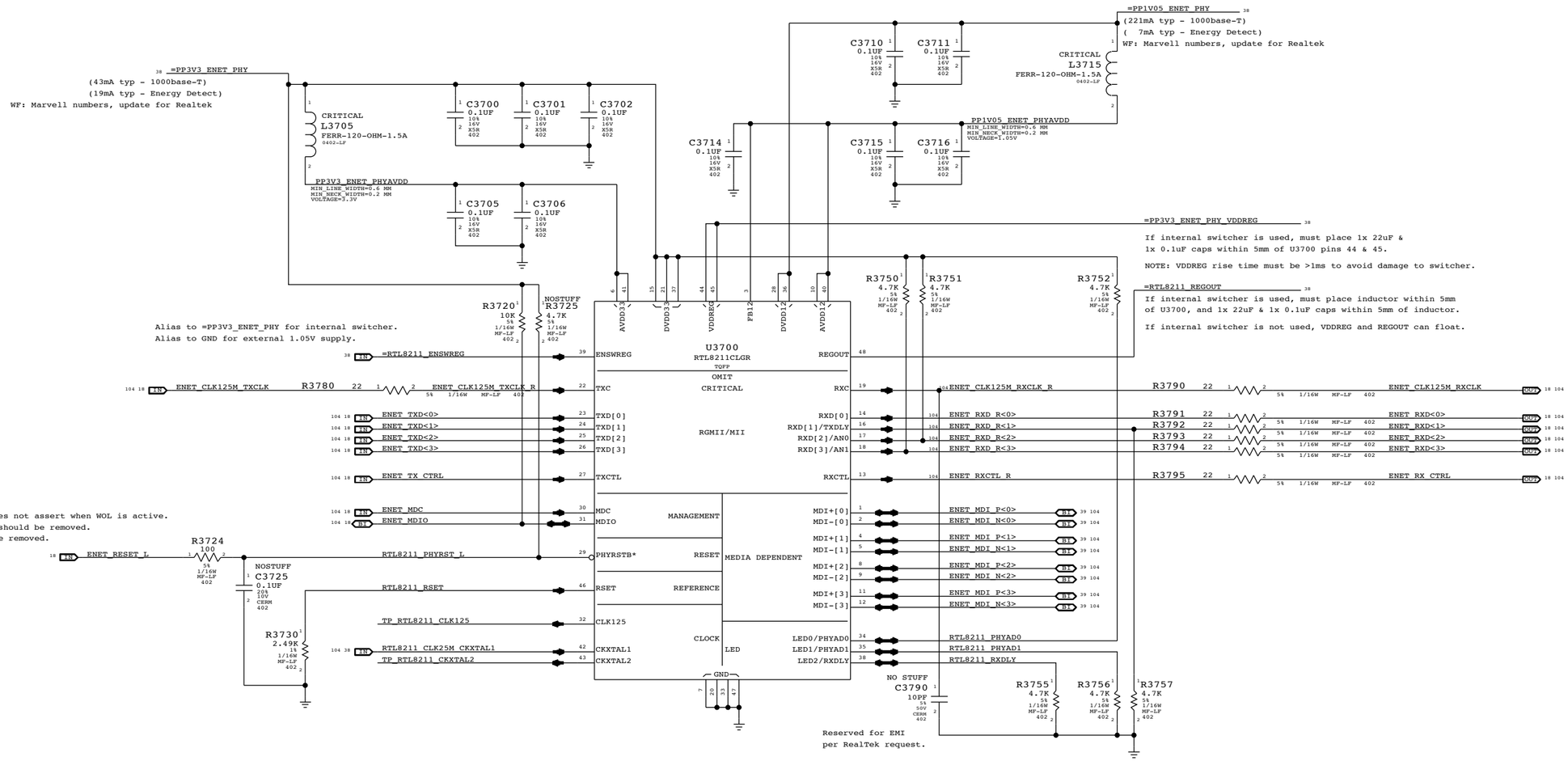

Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC MASTER=K51 SYNC DATE=12/08/2008

PAGE TITLE
Ethernet PHY (RTL8211CL)

Apple Inc.

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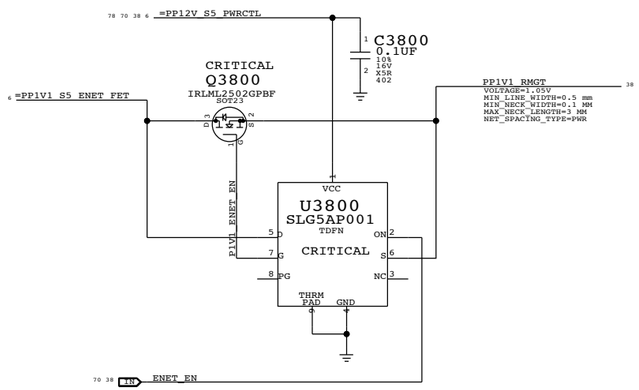
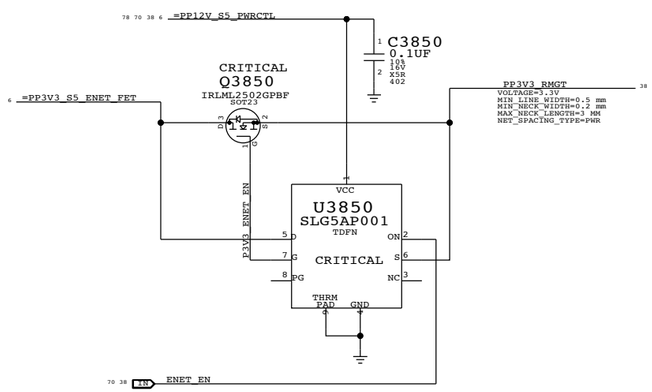
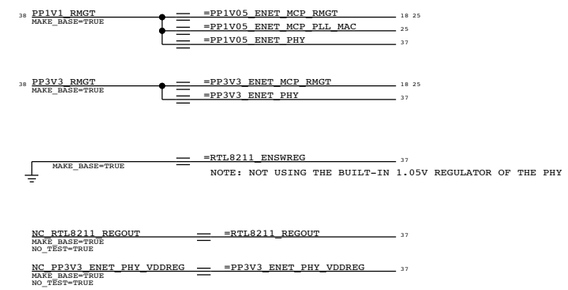
1.1V ENET FET



3.3V ENET FET

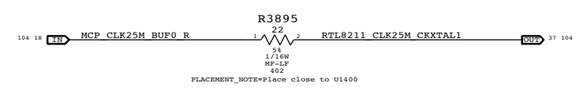


ENET ALIASES



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



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PAGE TITLE

Ethernet Support

Apple Inc.

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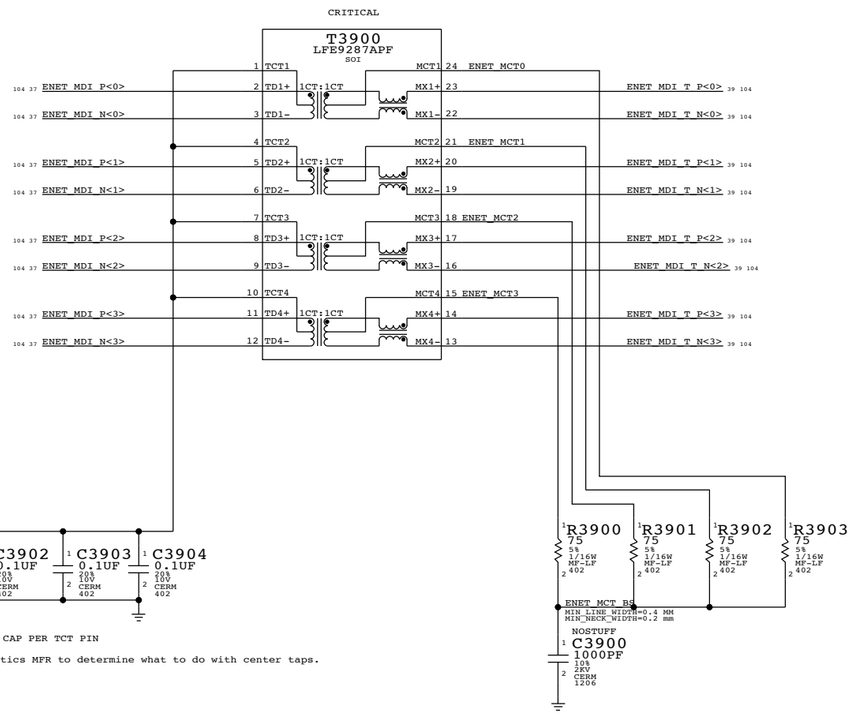

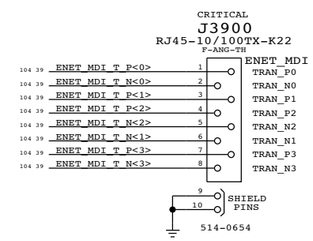

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PAGE TITLE

ETHERNET CONNECTOR

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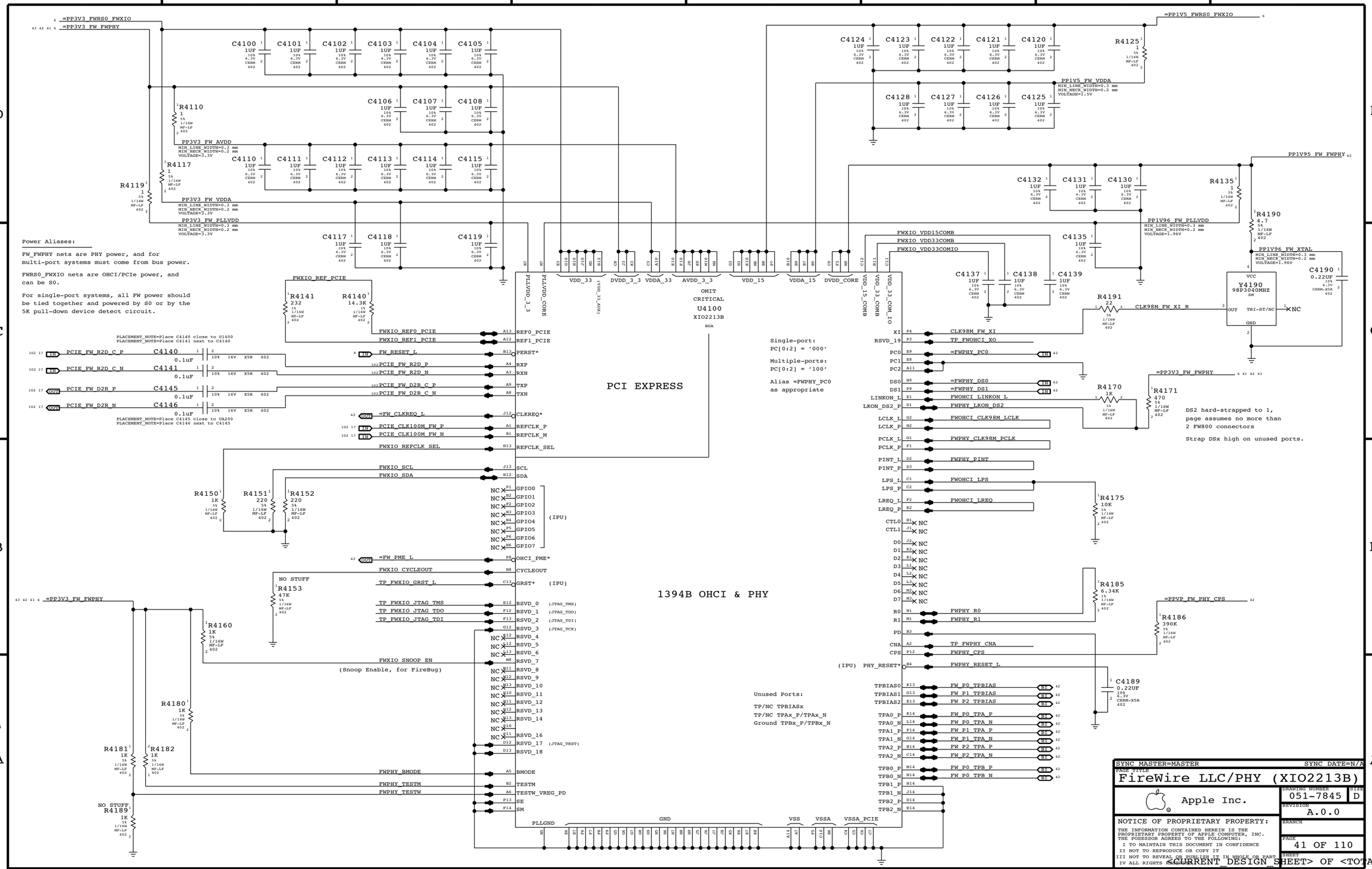

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PAGE TITLE
FireWire LLC/PHY (XIO2213B)

Apple Inc.

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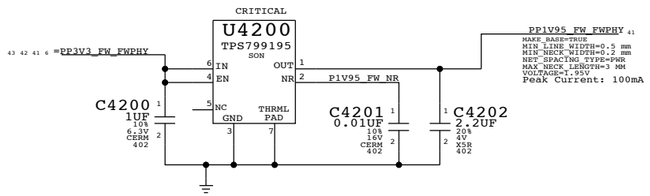
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity

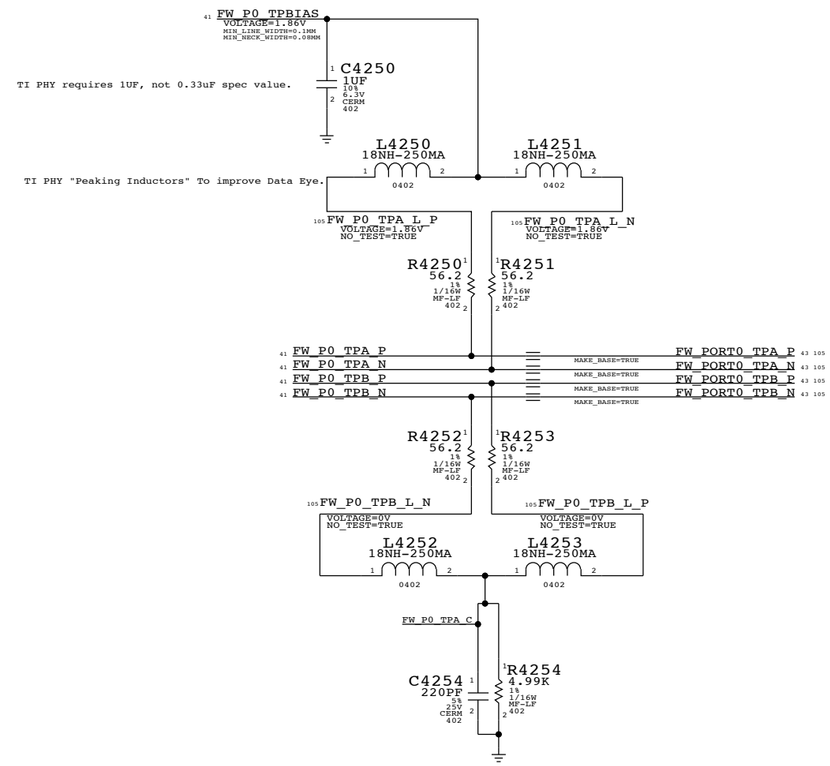
41 =FW_CLKREQ_L — FW_CLKREQ_L 17
MAKE_BASE=TRUE

41 =FW_PME_L — FW_PME_L 19
MAKE_BASE=TRUE

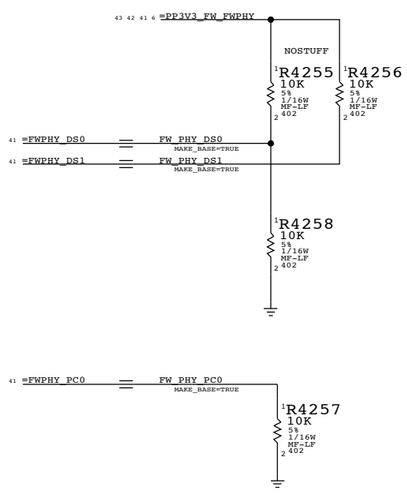
41 =PPVP_FW_PHY_CPS — PPVP_FW_PHY_CPS 43
MAKE_BASE=TRUE

Termination

Place close to FireWire PHY



1394 PHY STRAPPING OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

iMacs are now one port only and have Power Code "000"

2ND & 3RD TPA/TPB PAIR UNUSED

41 FW_P1_TPBIAS — NC_FW_PORT1_TPBIAS
MAKE_BASE=TRUE
NO_TEST=TRUE

41 FW_P1_TPA_P — NC_FW_PORT1_TPA_P
MAKE_BASE=TRUE
NO_TEST=TRUE

41 FW_P1_TPA_N — NC_FW_PORT1_TPA_N
MAKE_BASE=TRUE
NO_TEST=TRUE

41 FW_P2_TPBIAS — NC_FW_PORT2_TPBIAS
MAKE_BASE=TRUE
NO_TEST=TRUE

41 FW_P2_TPA_P — NC_FW_PORT2_TPA_P
MAKE_BASE=TRUE
NO_TEST=TRUE

41 FW_P2_TPA_N — NC_FW_PORT2_TPA_N
MAKE_BASE=TRUE
NO_TEST=TRUE

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FW: 1394B MISC

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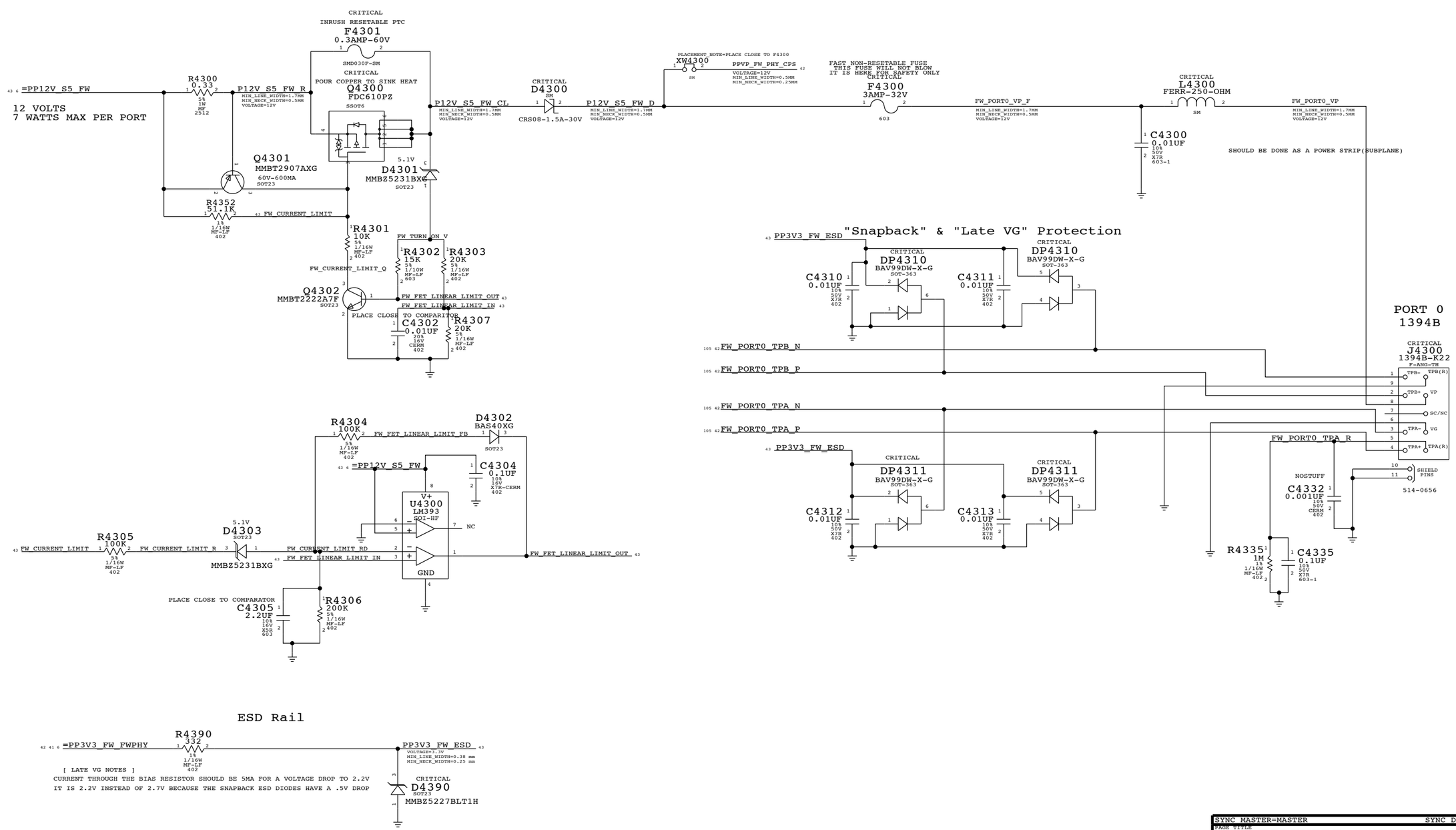

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FIREWIRE CONNECTOR

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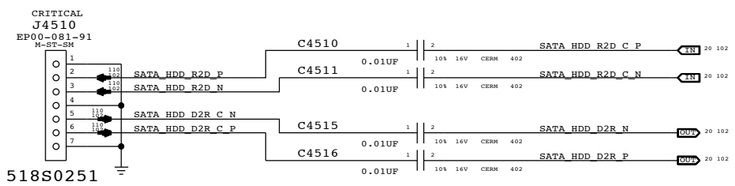
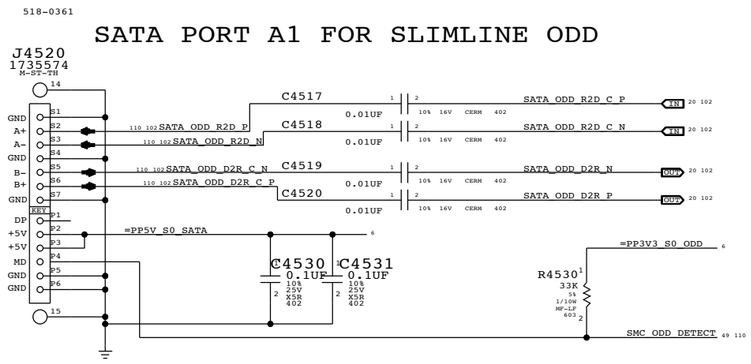
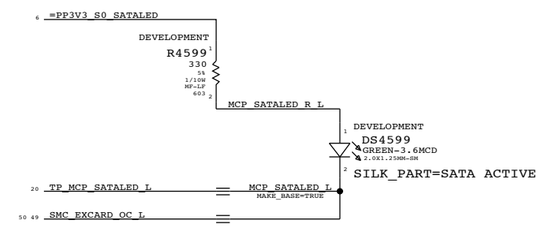
SATA PORT A0 FOR HDD



SATA PORT A1 FOR SLIMLINE ODD



SATA Activity LED



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

SATA Connectors

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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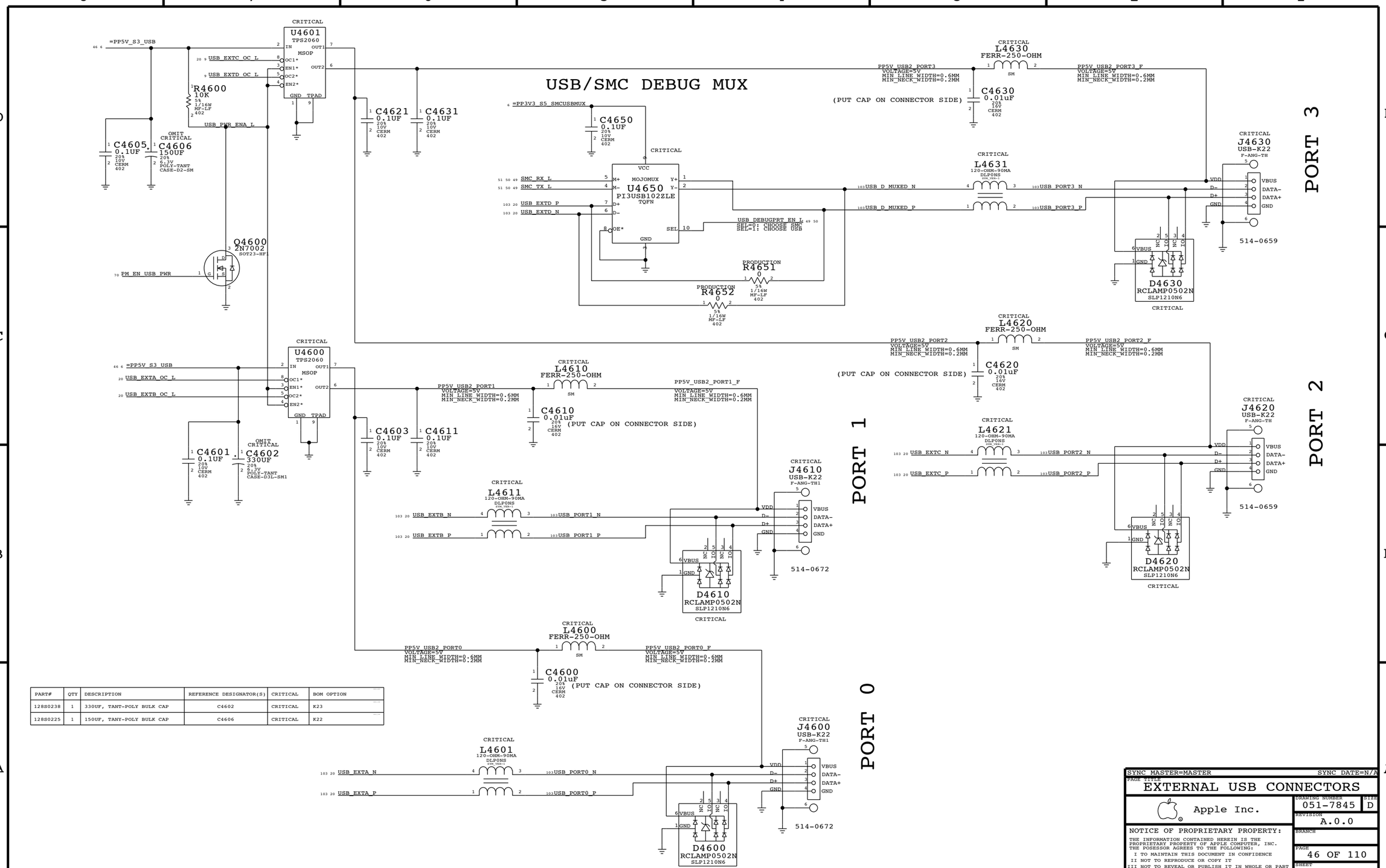

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0238	1	330UF, TANT-POLY BULK CAP	C4602	CRITICAL	K23
128S0225	1	150UF, TANY-POLY BULK CAP	C4606	CRITICAL	K22

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

EXTERNAL USB CONNECTORS

Apple Inc.

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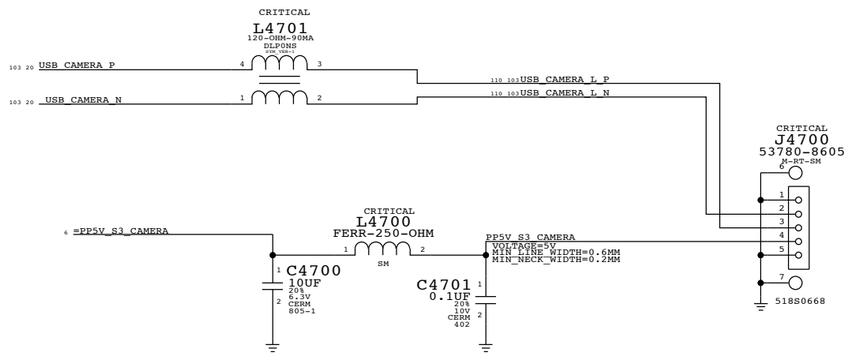
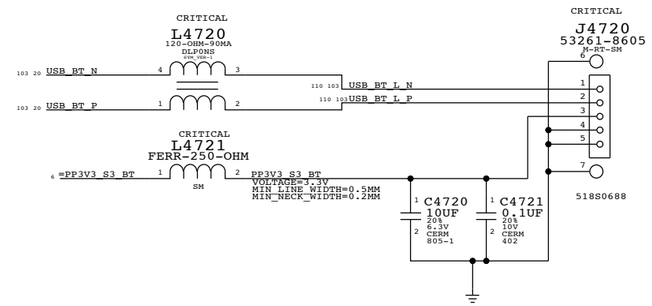
CAMERA CONNECTOR & FILTER

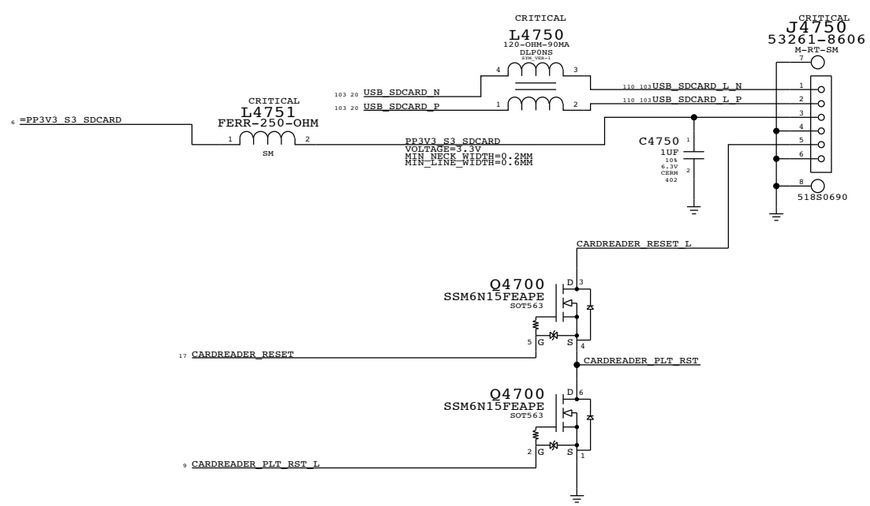


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

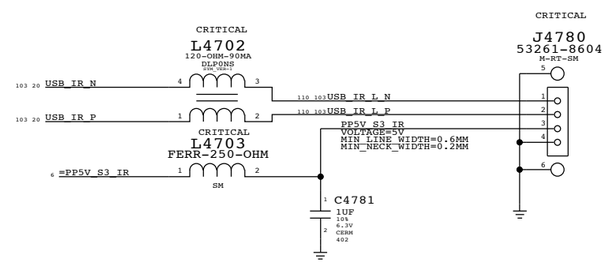
K37L (BLUETOOTH) CONNECTOR



SD Card Reader Board Connector



IR RECEIVER CONNECTOR



SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE
Internal USB Connections

Apple Inc.

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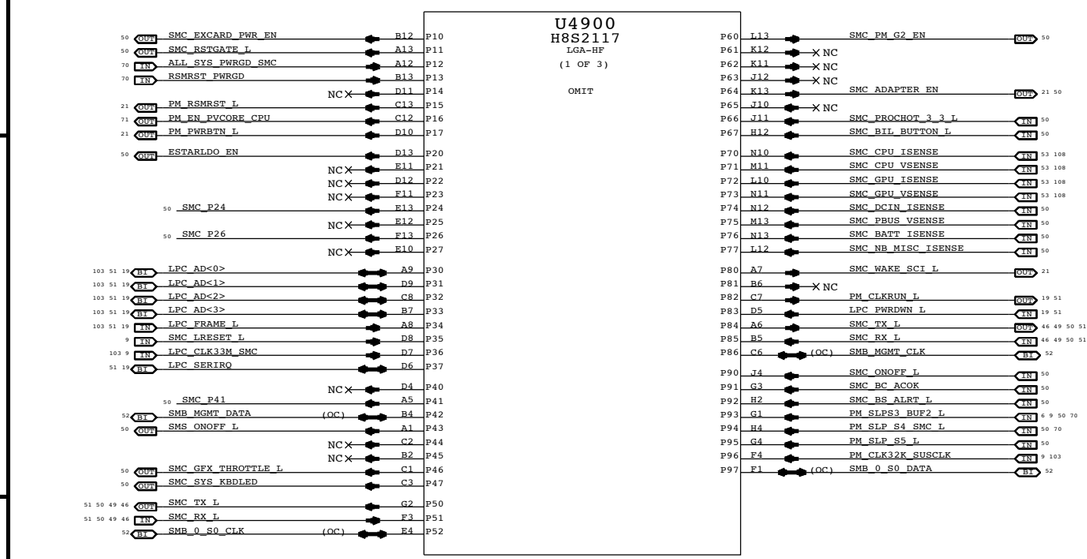
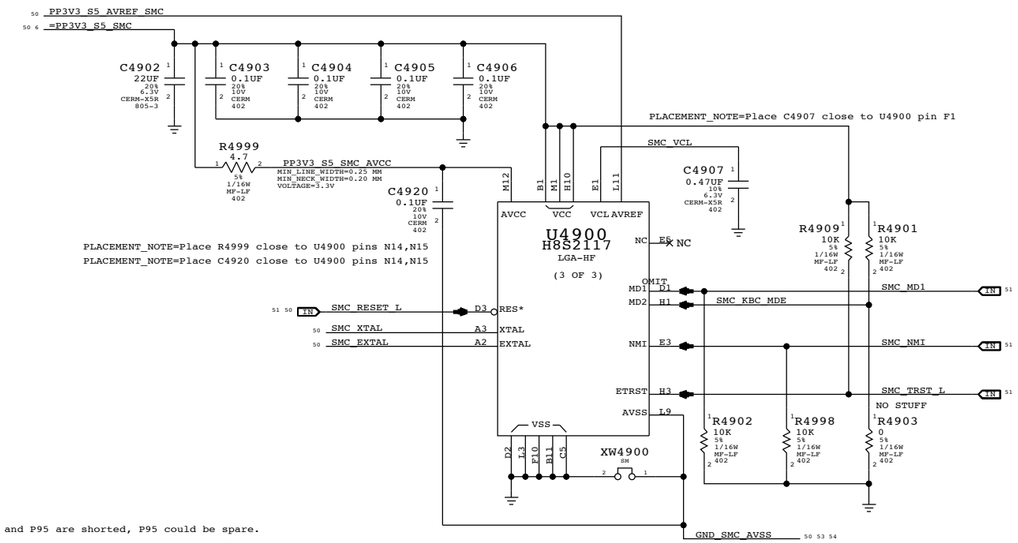
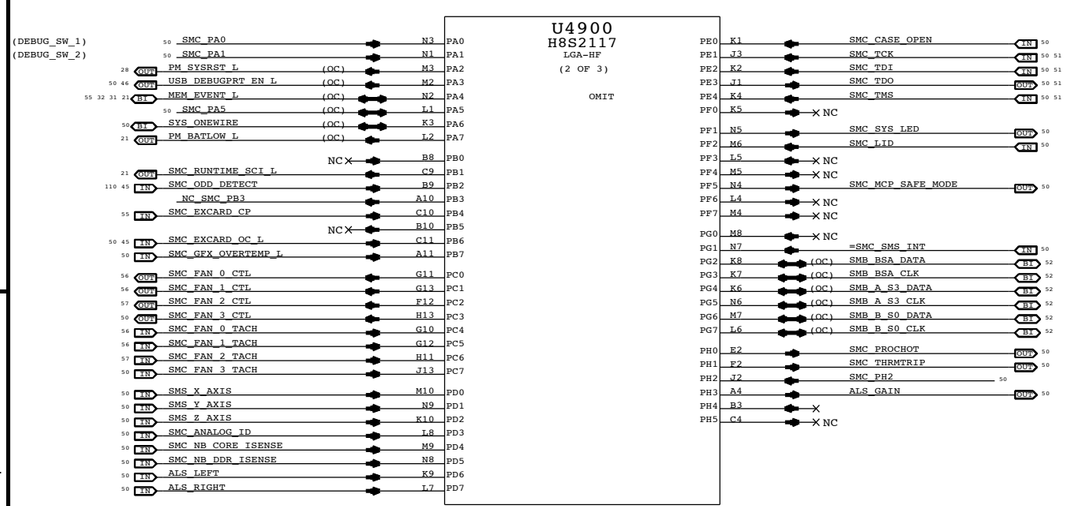
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC MASTER=MASTER	SYNC DATE=N/A
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER: 051-7845 SIZE: D
	REVISION: A.0.0
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	PAGE: 49 OF 110
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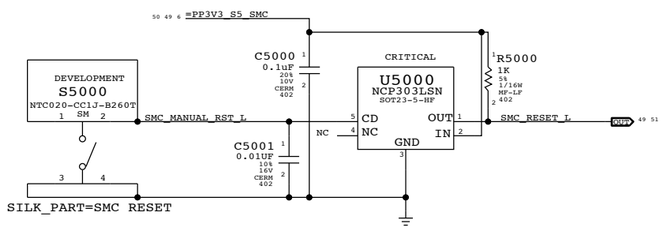
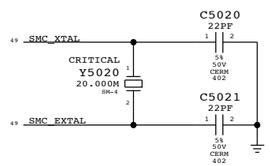
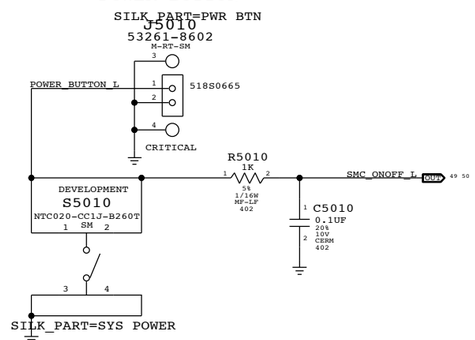
SMC Reset Button / Brownout Detect



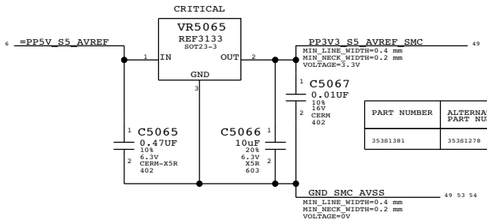
SMC Crystal Circuit



POWER BUTTON

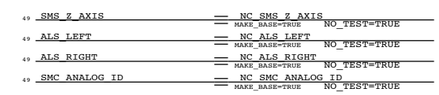


SMC AVREF Supply

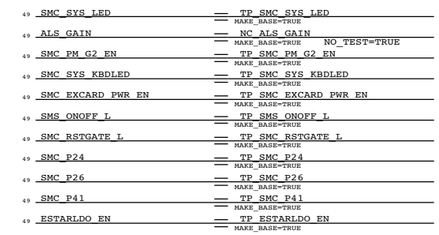


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Intersil ISL69002-33

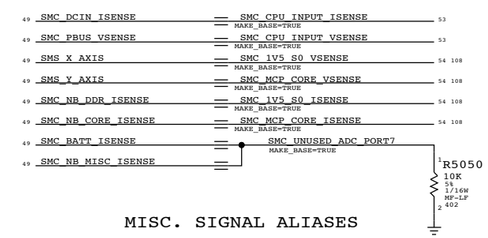
UNUSED TP/NC ALIASES - PORT D - INTERNAL PULLUPS



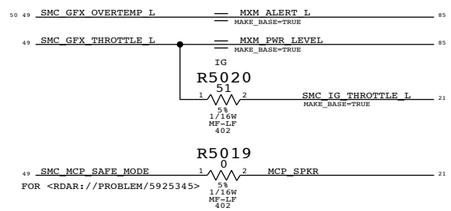
UNUSED TP/NC ALIASES

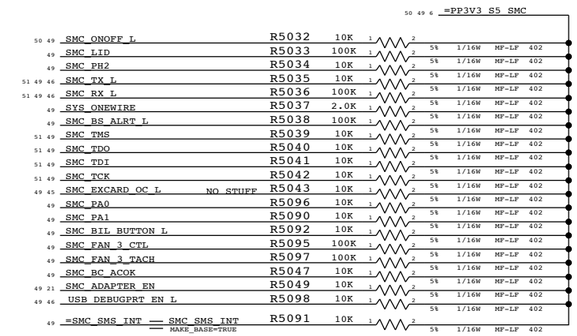


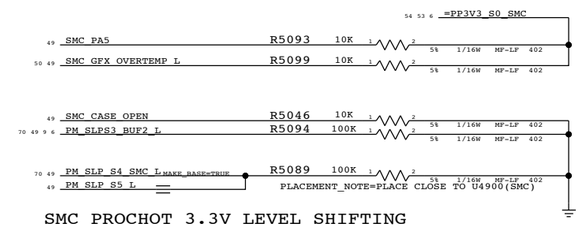
ANALOG SENSORS



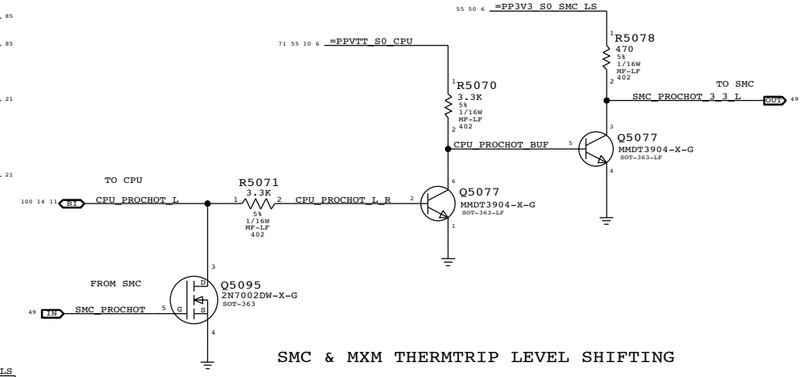
MISC. SIGNAL ALIASES



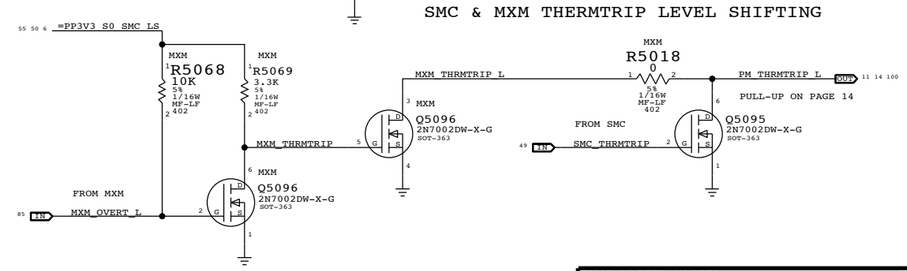




SMC PROCHOT 3.3V LEVEL SHIFTING



SMC & MXM THERMTRIP LEVEL SHIFTING



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

SMC Support

Apple Inc.

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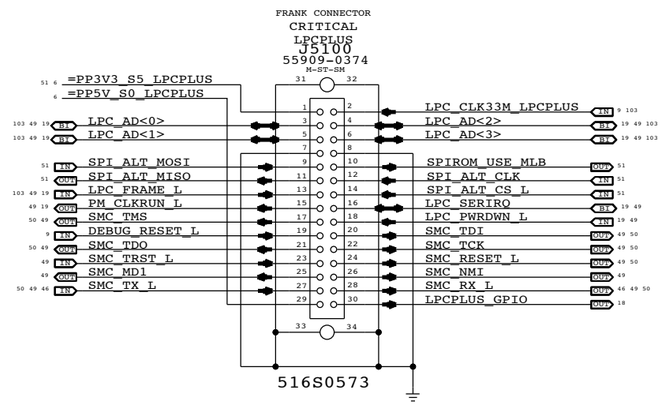
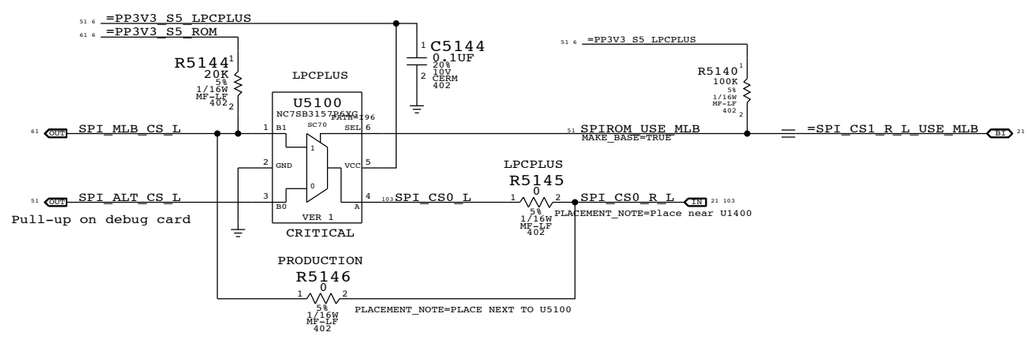
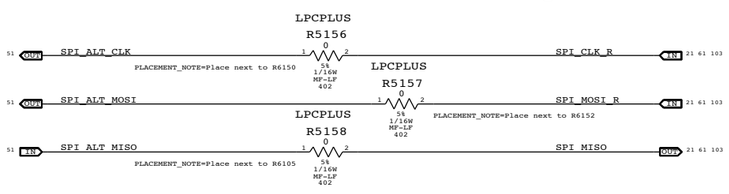
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



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PAGE TITLE
LPC+SPI Debug Connector

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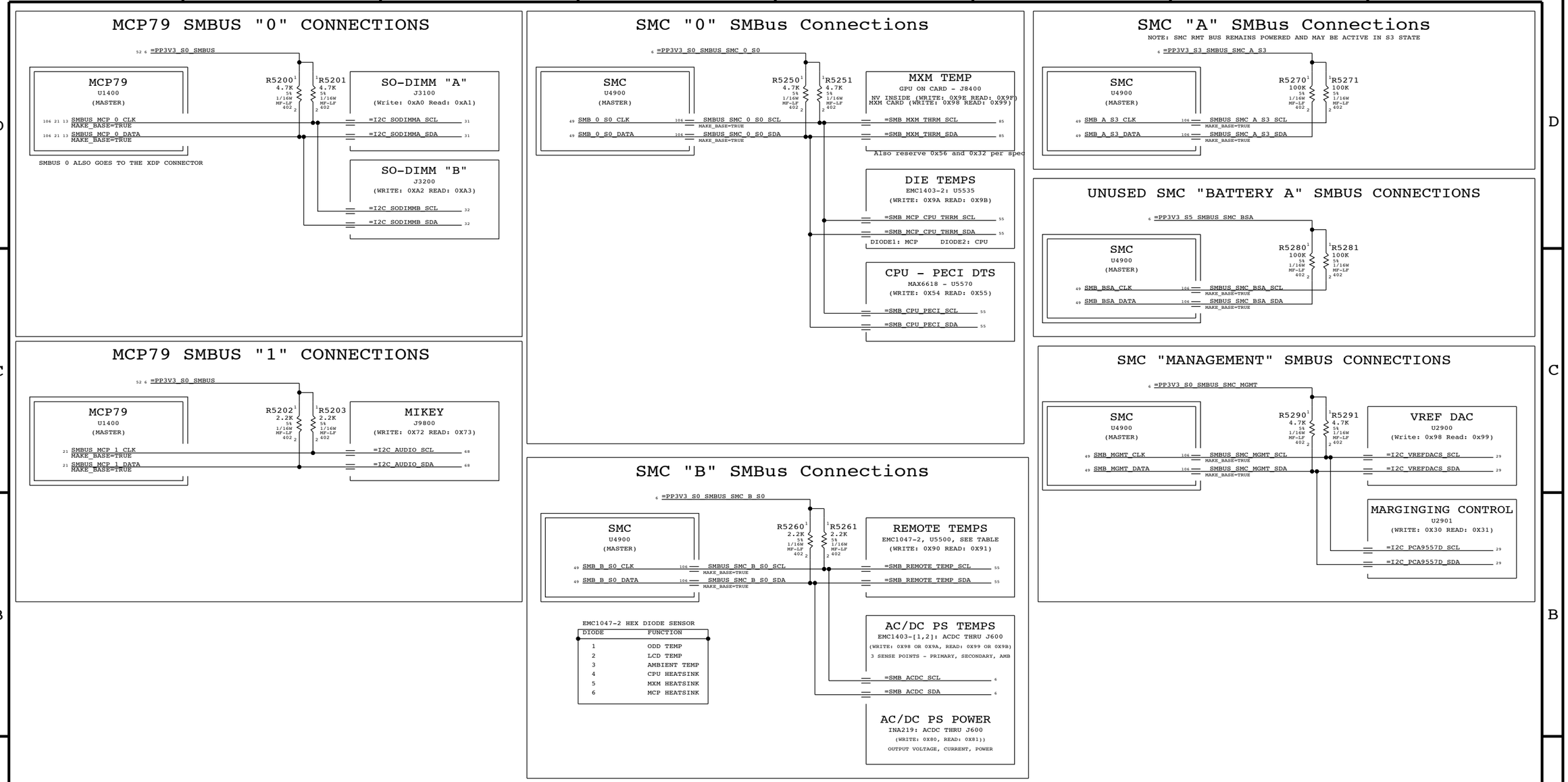

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PAGE TITLE

SMBUS CONNECTIONS

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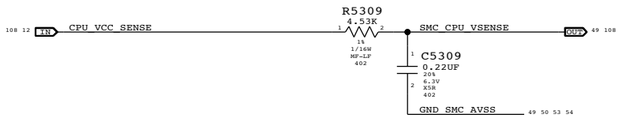
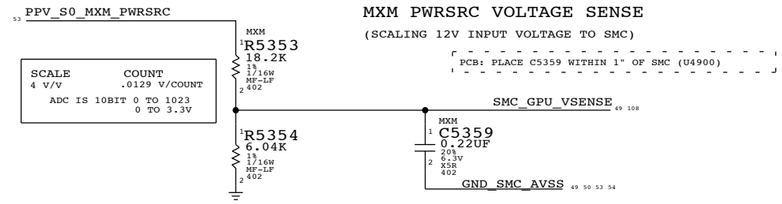
CPU Voltage Sense / Filter



Place RC close to SMC

MXM PWRSRC VOLTAGE SENSE

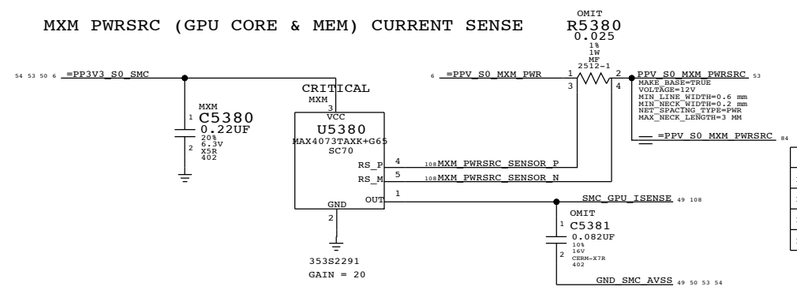
(SCALING 12V INPUT VOLTAGE TO SMC)



SCALE	COUNT
4 V/V	.0129 V/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



K50 SET FOR APPROX 2V AT 4A ON PWRSRC

SCALE	COUNT
2 A/V	.0064453 A/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

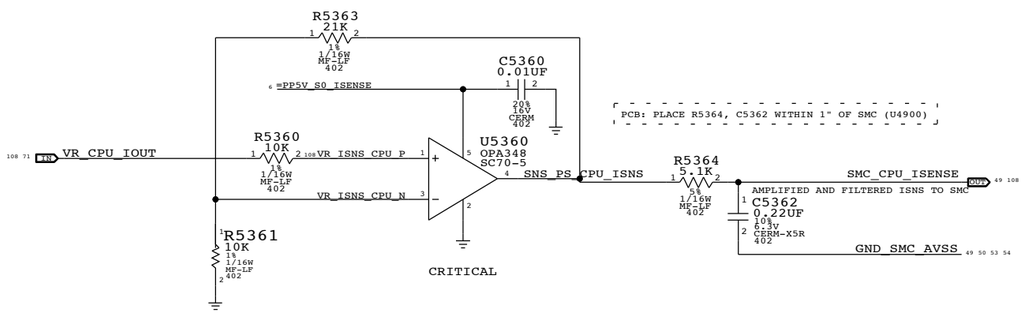
K51 SET FOR APPROX 1.98V AT 5.5A ON PWRSRC

SCALE	COUNT
2.778 A/V	.0087518 A/COUNT

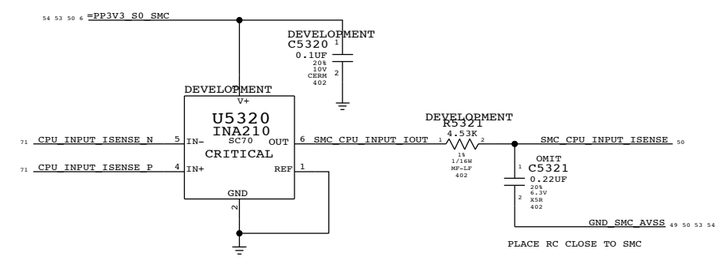
ADC IS 10BIT 0 TO 1023
0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	K22_MXM
107S0111	1	18 MILLIOHM	R5380	CRITICAL	K23_MXM
132S0242	1	CAP,0.082UF,402	C5381		MXM
116S0090	1	RES,10KOHM,5%,402	C5381		IG

CPU CURRENT SENSE AMP & FILTER

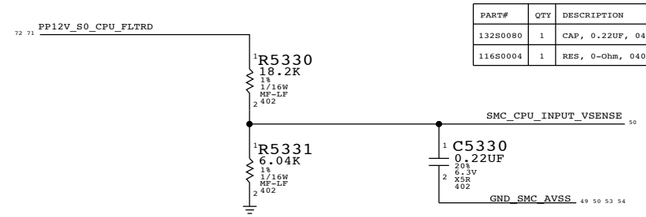


CPU CORE INPUT SIDE CURRENT & VOLTAGE SENSE



PLACE RC CLOSE TO SMC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 0402	C5321		DEVELOPMENT
116S0004	1	RES, 0-Ohm, 0402	C5321		PRODUCTION



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
CPU/MXM CURRENT AND VOLTAGE SENSE

Apple Inc.

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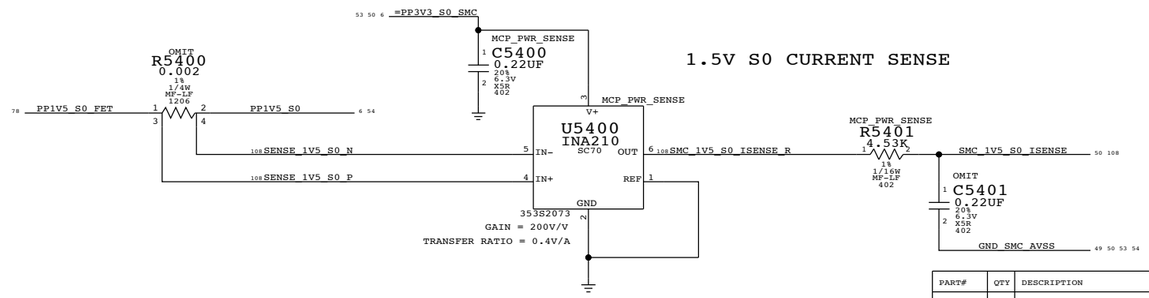
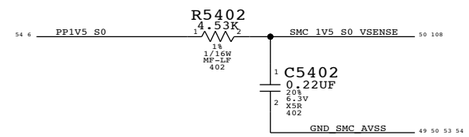
1.5V S0 CURRENT SENSE



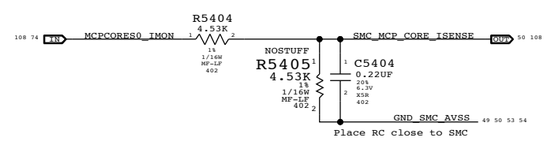
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5400	CRITICAL	MCP_PWR_SENSE
101S0414	1	RES,0 OHM,1206,20MILLIOHM MAX	R5400	CRITICAL	PRODUCTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 0402	C5401		MCP_PWR_SENSE
116S0004	1	RES, 0 OHM, 0402	C5401		PRODUCTION

1.5V S0 VOLTAGE SENSE

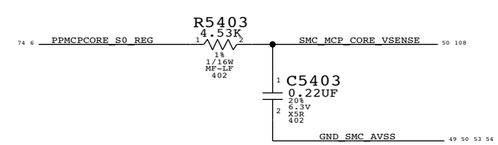


MCP CORE CURRENT SENSE



SCALE IS 0.116 V/A

MCP CORE VOLTAGE SENSE



SYNC MASTER=K51 SYNC DATE=12/08/2008

PAGE TITLE
MCP CURRENT AND VOLTAGE SENSE

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

REVISION A.0.0

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PAGE 54 OF 110

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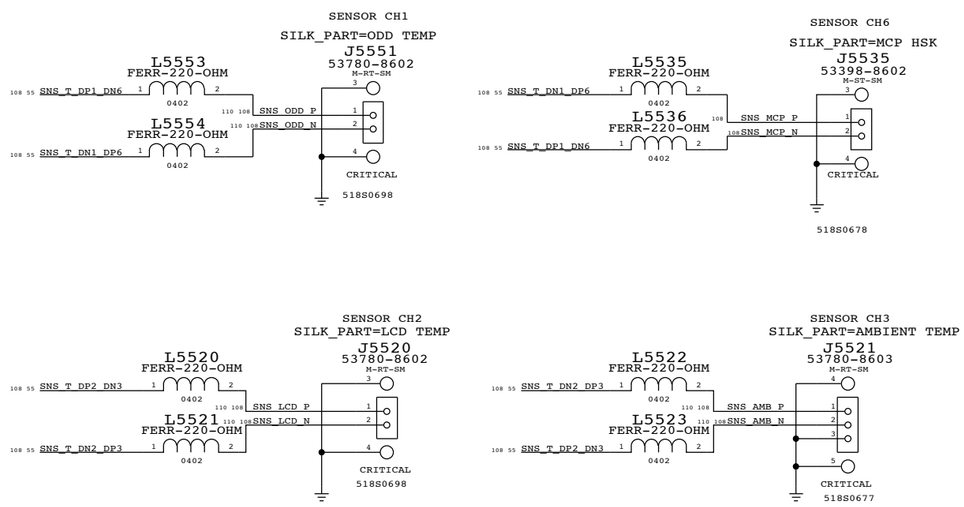
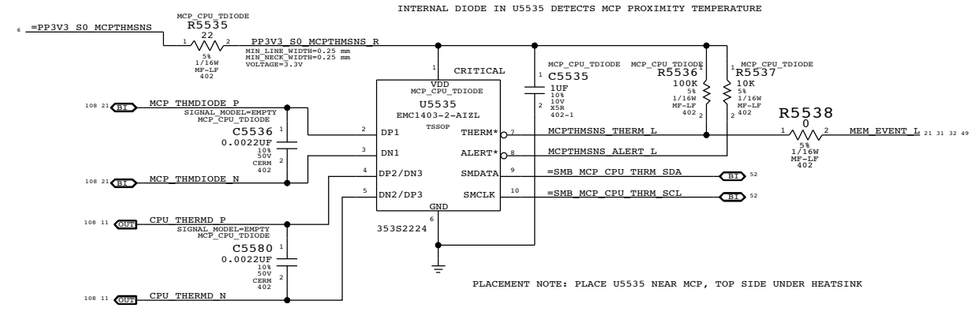
REMOTE THERMAL SENSORS

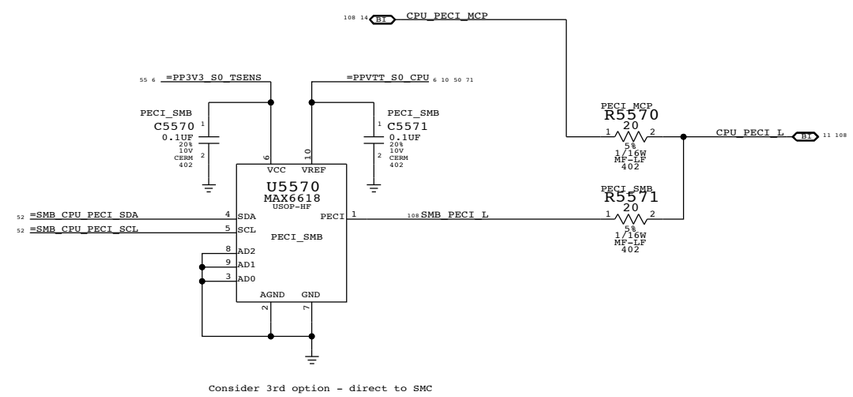
HEATSINKS, AMBIENT, PANEL AND ODD



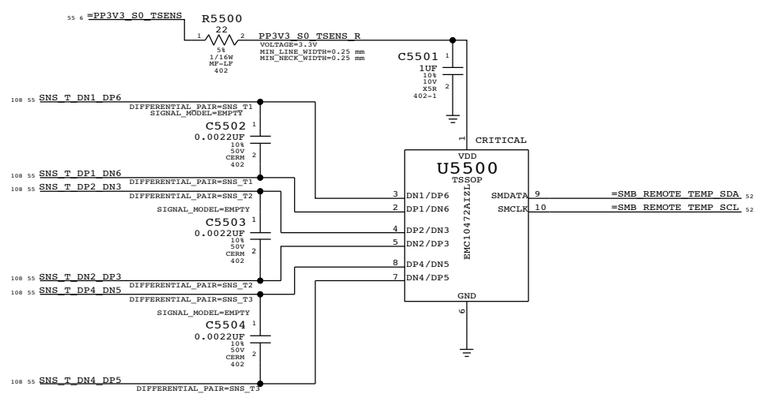
MCP & CPU T-Diode Thermal Sensor



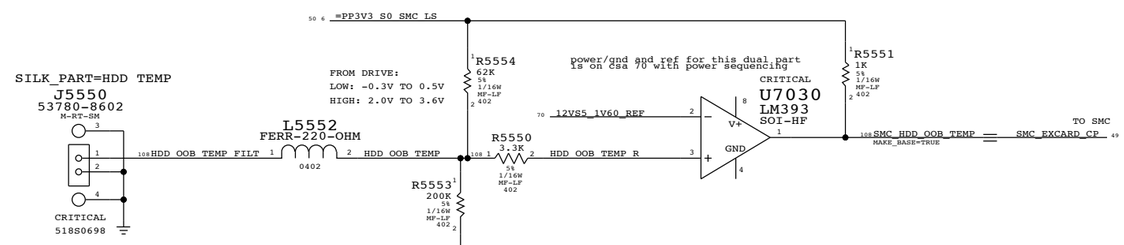
CPU PECI DTS OPTIONS



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



Drive active = valid signal protocol
Drive asleep = HDD drives HDD_OOB_TEMP low
Drive disconnected = pulled high

Cannot pull low because some drives use this bit to determine 1.5 Gbps vs. 3.0 Gbps SATA

Must pull high to 2.5V for compatibility with all drives

SYNC MASTER=MASTER	SYNC DATE=N/A
PAGE TITLE: Thermal Sensors	
Apple Inc.	DRAWING NUMBER: 051-7845 SIZE: D
	REVISION: A.0.0
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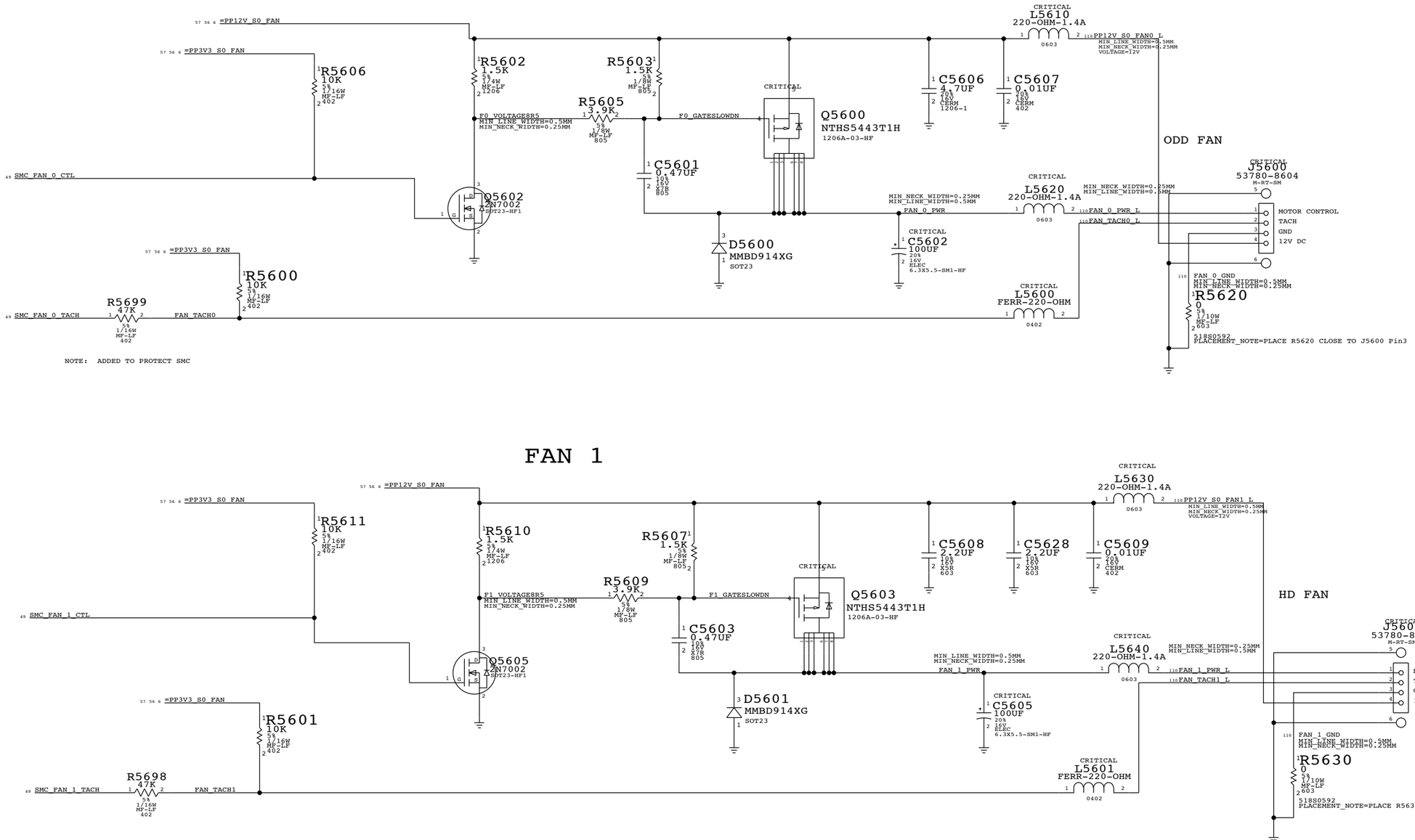
	PAGE: 55 OF 110
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: HD AND OD FAN

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DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

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PAGE: 56 OF 110

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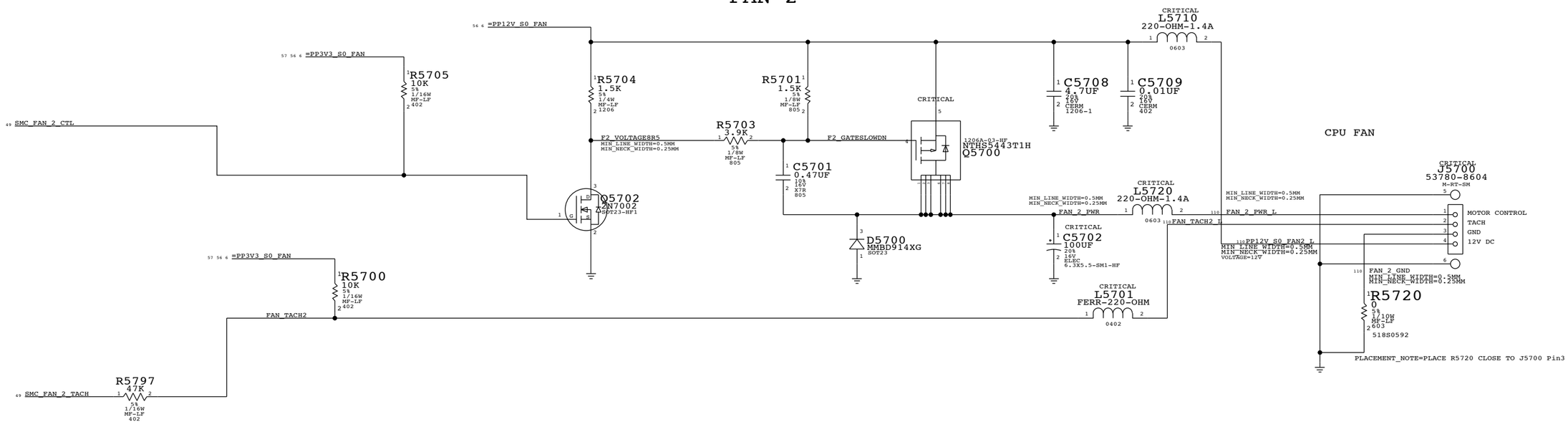
FAN 2



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

CPU FAN

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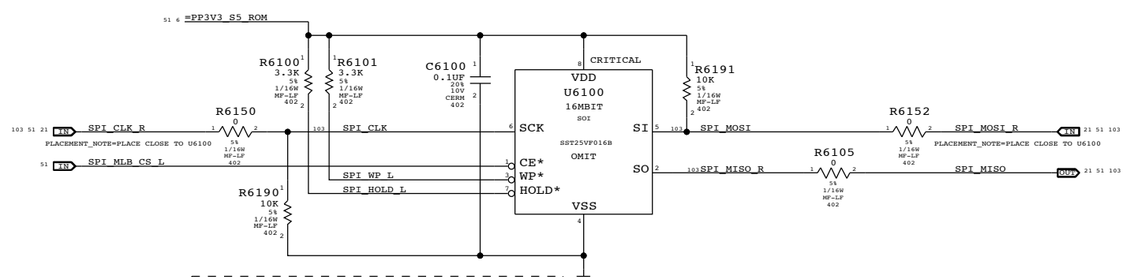

MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: MCP79 only issues 'READ' (0x03) commands not 'READ_FAST' (0x0B). Limits SPI bus frequency and part selection.

SST25VF016B max speed for READ command is 25MHz.

SYNC MASTER=K51 SYNC DATE=12/08/2008

PAGE TITLE

SPI ROM

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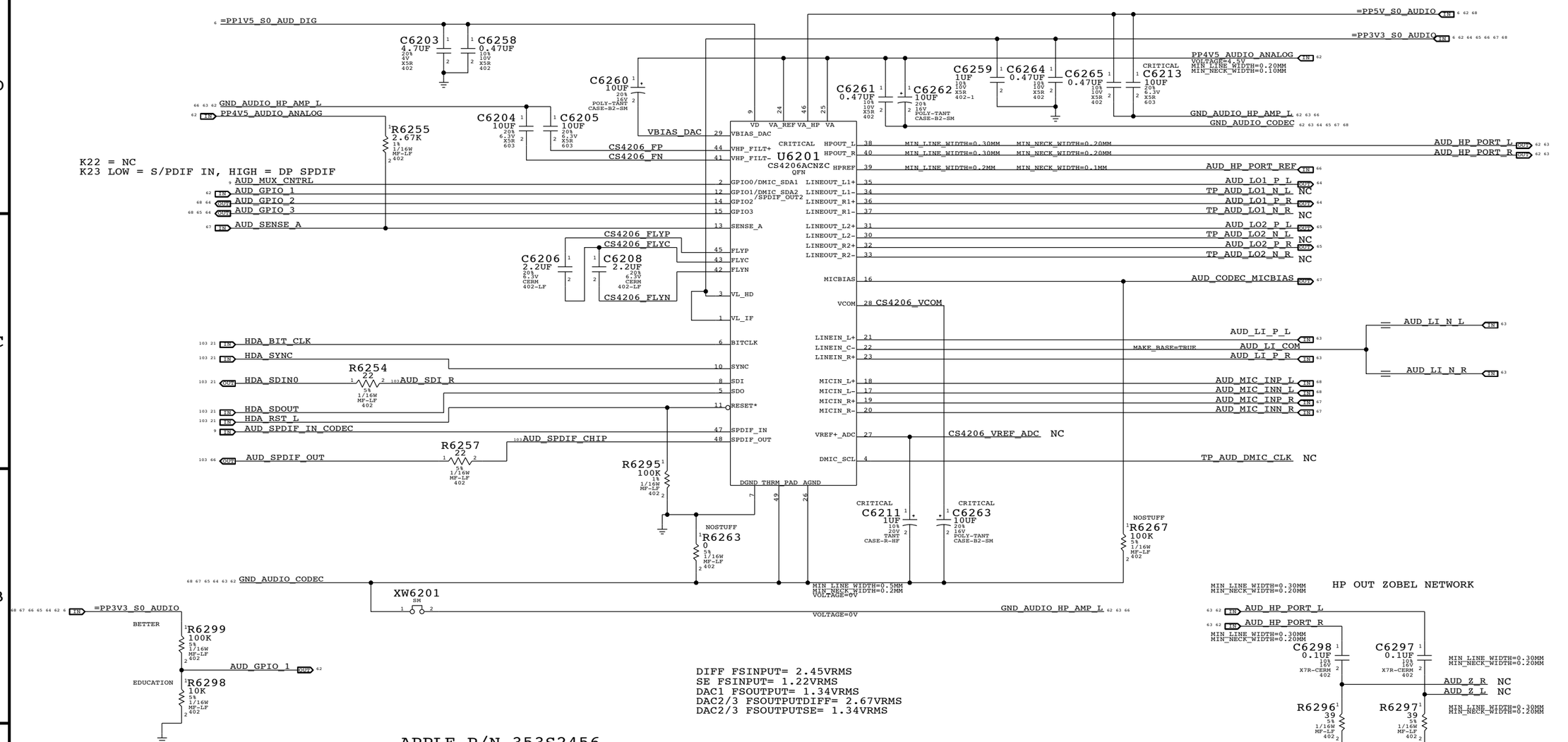
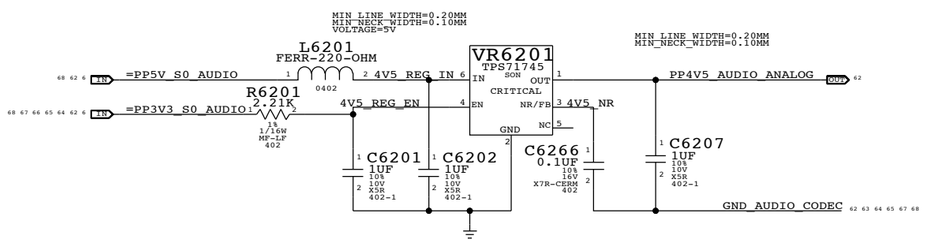
AUDIO CODEC
APPLE P/N 353S2592



APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC



SYNC MASTER=SKIPAUDIO SYNC DATE=06/01/2009

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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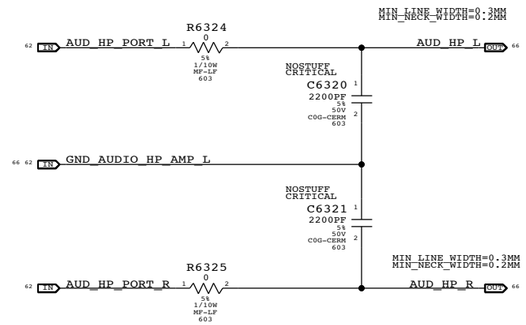
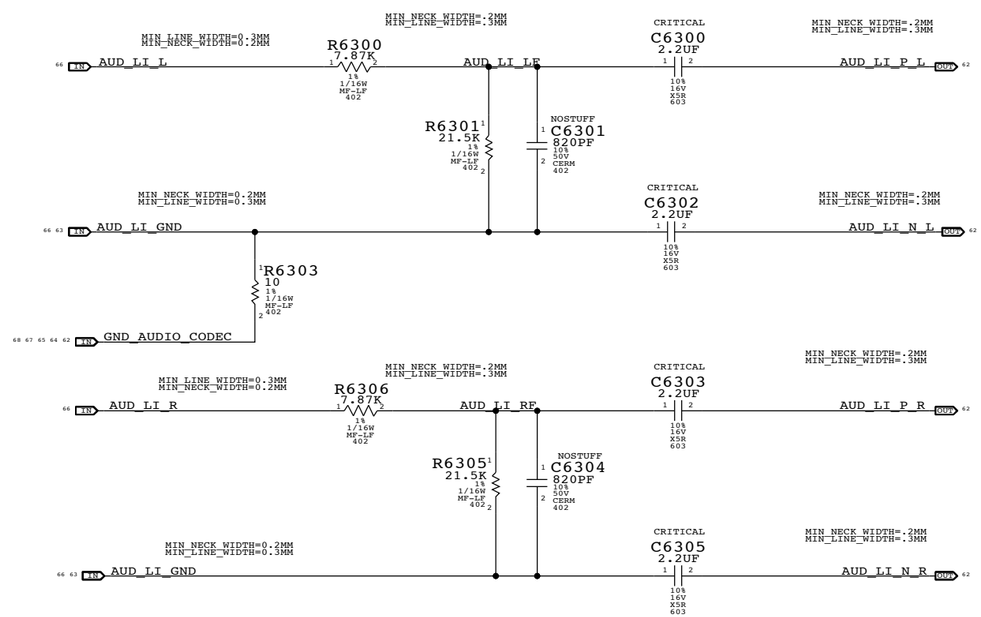
1ST ORDER DAC FILTER PLACEHOLDER



CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC MASTER=SKIPAUDIO SYNC DATE=06/01/2009

PAGE TITLE
AUDIO: FILTER/BUFFER

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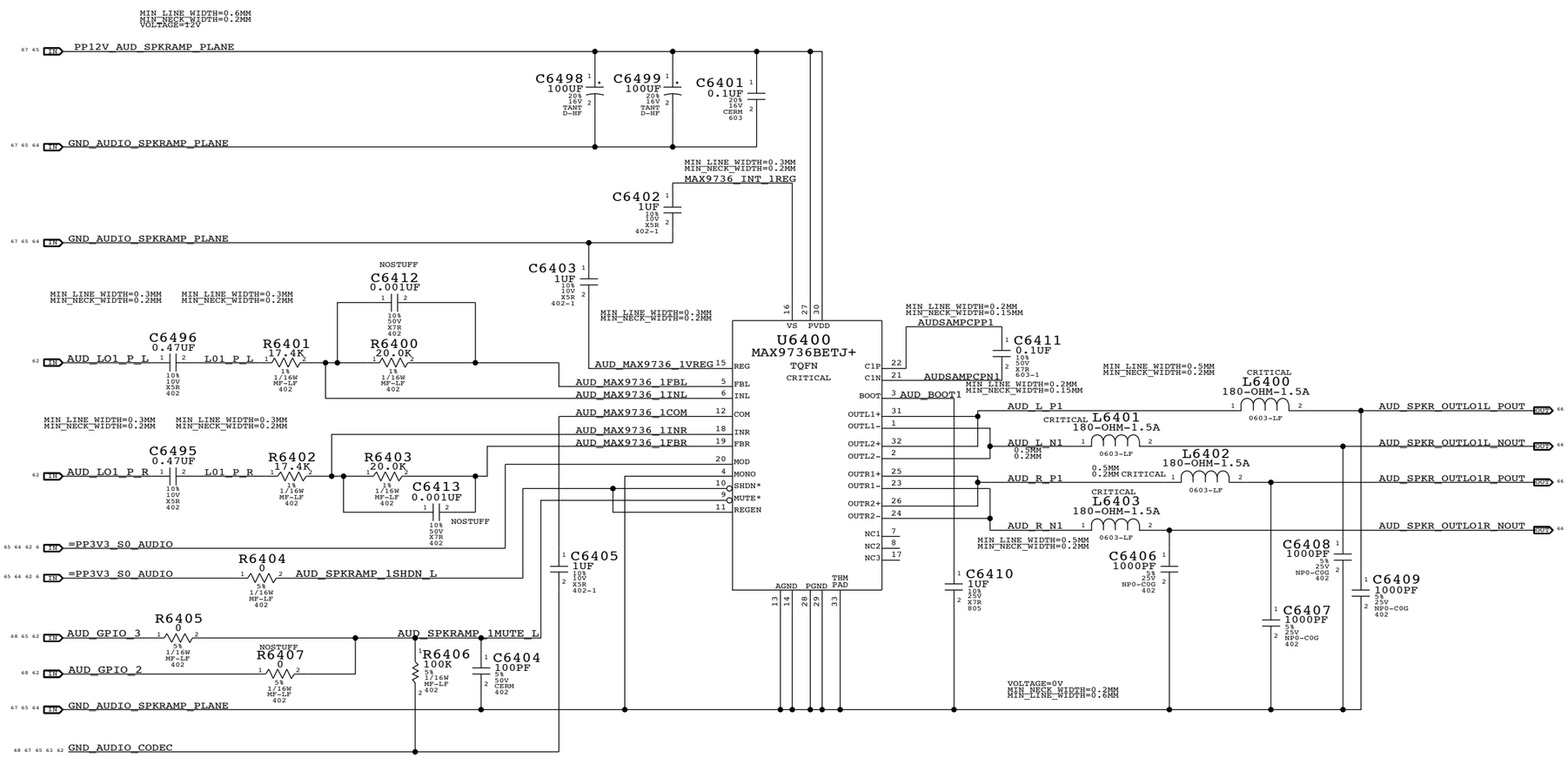
TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ

POUT = 6.76 W INTO 8 OHMS @ 1% THD+N



SYNC MASTER=SKIPAUDIO SYNC DATE=06/01/2009

PAGE TITLE
AUDIO: SPEAKER AMP

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WOOFER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
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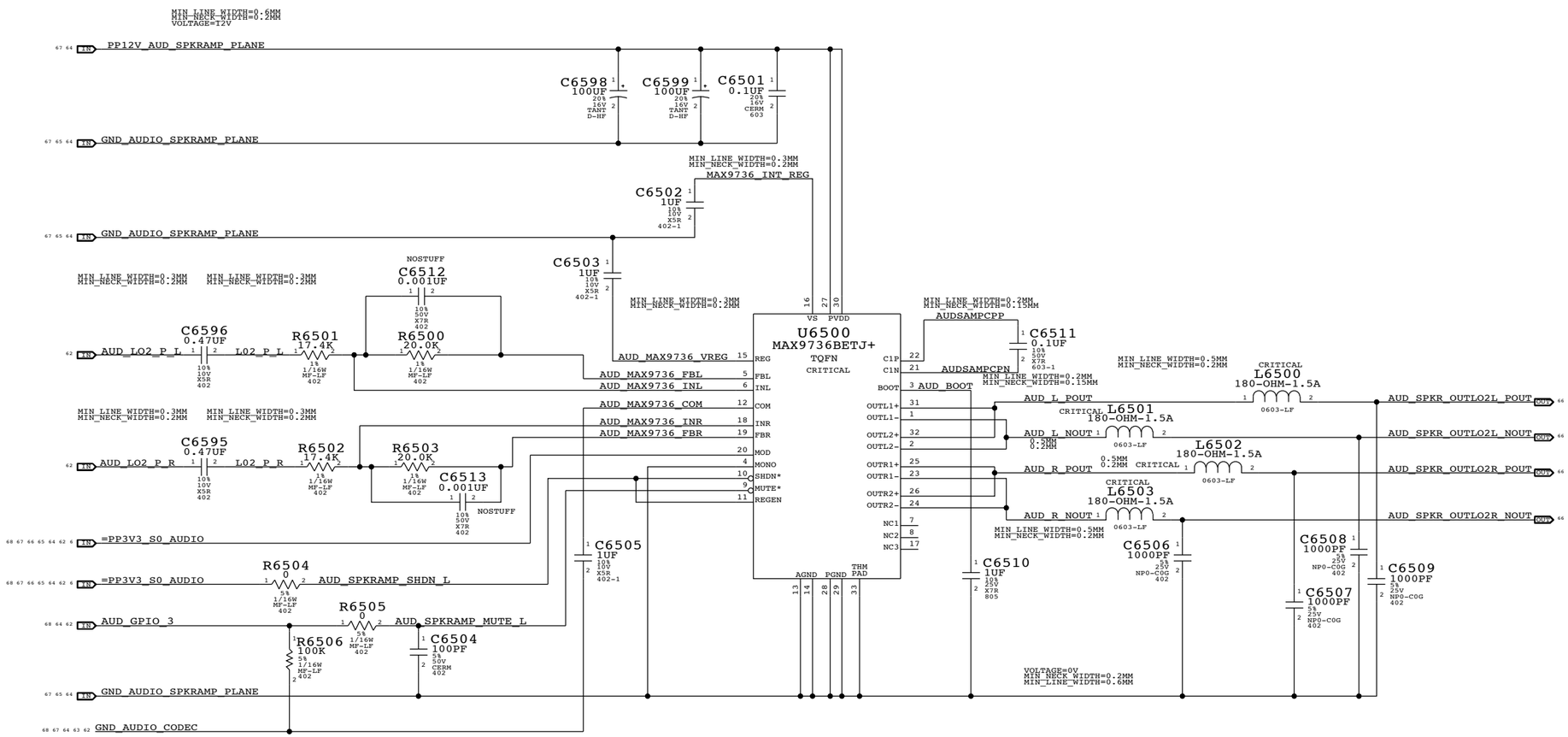

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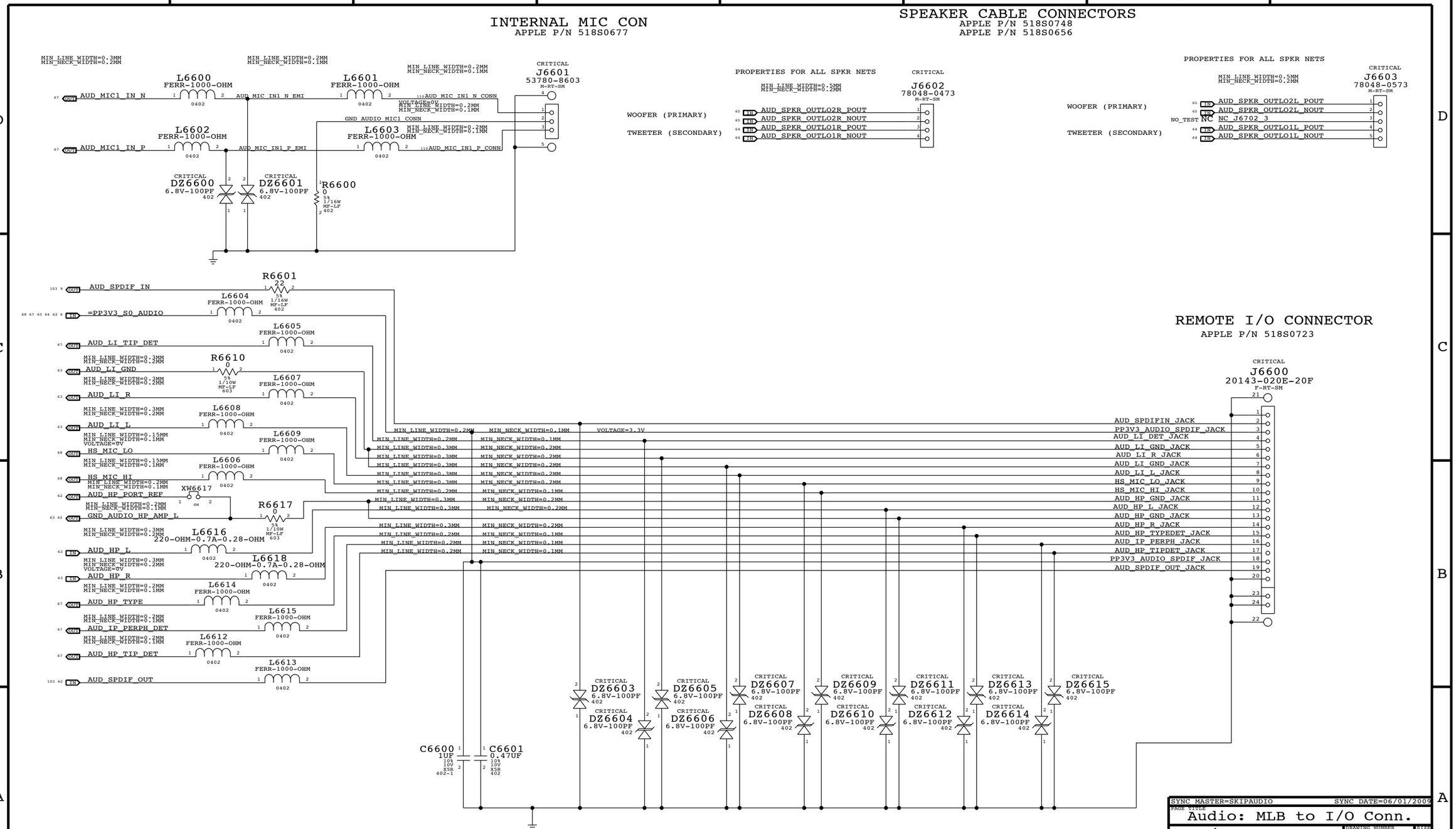
INTERNAL MIC CON
APPLE P/N 518S0677
SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656
REMOTE I/O CONNECTOR
APPLE P/N 518S0723
J6601 53780-8603
J6602 78048-0473
J6603 78048-0573
J6600 20143-020E-20F
L6600 FERR-1000-OHM
L6601 FERR-1000-OHM
L6602 FERR-1000-OHM
L6603 FERR-1000-OHM
DZ6600 6.8V-100PF
DZ6601 6.8V-100PF
R6600 0
R6601 22
L6604 FERR-1000-OHM
L6605 FERR-1000-OHM
R6610 0
L6607 FERR-1000-OHM
L6608 FERR-1000-OHM
L6609 FERR-1000-OHM
L6606 FERR-1000-OHM
XW6617
R6617 0
L6616 220-OHM-0.7A-0.28-OHM
L6618 220-OHM-0.7A-0.28-OHM
L6614 FERR-1000-OHM
L6615 FERR-1000-OHM
L6612 FERR-1000-OHM
L6613 FERR-1000-OHM
DZ6603 6.8V-100PF
DZ6604 6.8V-100PF
DZ6605 6.8V-100PF
DZ6606 6.8V-100PF
DZ6607 6.8V-100PF
DZ6608 6.8V-100PF
DZ6609 6.8V-100PF
DZ6610 6.8V-100PF
DZ6611 6.8V-100PF
DZ6612 6.8V-100PF
DZ6613 6.8V-100PF
DZ6614 6.8V-100PF
DZ6615 6.8V-100PF
C6600 1UF
C6601 0.47UF
AUD_MIC1_IN_N
AUD_MIC1_IN_P
AUD_MIC_IN1_N_EMI
AUD_MIC_IN1_P_EMI
AUD_MIC_IN1_N_CONN
AUD_MIC_IN1_P_CONN
GND_AUDIO_MIC1_CONN
WOOFER (PRIMARY)
TWEETER (SECONDARY)
AUD_SPKR_OUTLO2R_POUT
AUD_SPKR_OUTLO2R_NOUT
AUD_SPKR_OUTLO1R_POUT
AUD_SPKR_OUTLO1R_NOUT
AUD_SPKR_OUTLO2L_POUT
AUD_SPKR_OUTLO2L_NOUT
NC_J6702_3
AUD_SPKR_OUTLO1L_POUT
AUD_SPKR_OUTLO1L_NOUT
PROPERTIES FOR ALL SPKR NETS
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUD_SPDIF_IN
=PP3V3_S0_AUDIO
AUD_LI_TIP_DET
AUD_LI_GND
AUD_LI_R
AUD_LI_L
HS_MIC_LO
HS_MIC_HI
AUD_HP_PORT_REF
GND_AUDIO_HP_AMP_L
AUD_HP_L
AUD_HP_R
AUD_HP_TYPE
AUD_IP_PERPH_DET
AUD_HP_TIP_DET
AUD_SPDIF_OUT
AUD_SPDIFIN_JACK
PP3V3_AUDIO_SPDIF_JACK
AUD_LI_DET_JACK
AUD_LI_GND_JACK
AUD_LI_R_JACK
AUD_LI_L_JACK
HS_MIC_LO_JACK
HS_MIC_HI_JACK
AUD_HP_GND_JACK
AUD_HP_L_JACK
AUD_HP_R_JACK
AUD_HP_TYPEDET_JACK
AUD_IP_PERPH_JACK
AUD_HP_TIPDET_JACK
AUD_SPDIF_OUT_JACK
VOLTAGE=3.3V
SYNC MASTER=SKIPAUDIO
SYNC DATE=06/01/2009
PAGE TITLE
Audio: MLB to I/O Conn.
Apple Inc.
DRAWING NUMBER
051-7845
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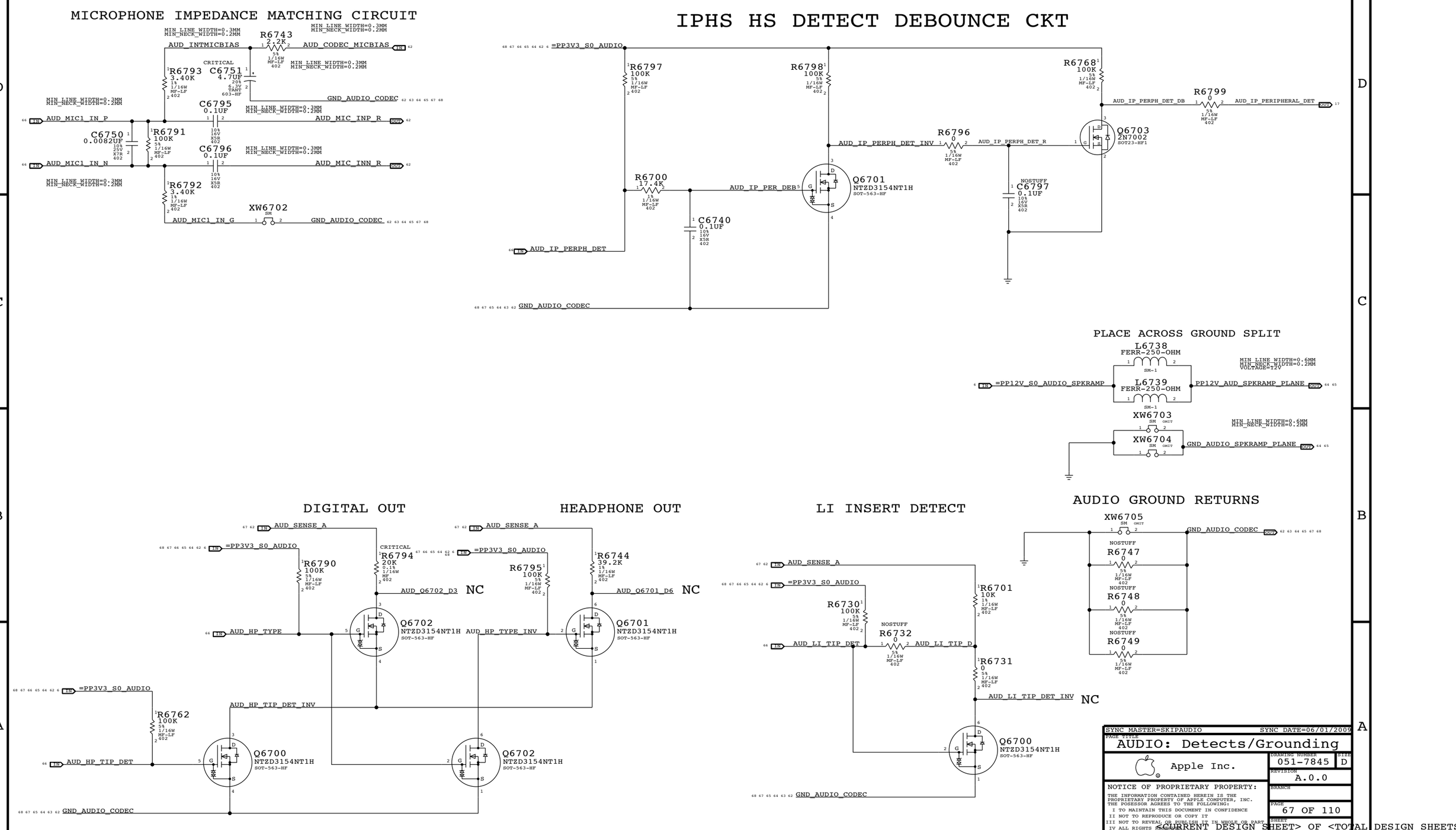
MICROPHONE IMPEDANCE MATCHING CIRCUIT
IPHS HS DETECT DEBOUNCE CKT
PLACE ACROSS GROUND SPLIT
DIGITAL OUT
HEADPHONE OUT
LI INSERT DETECT
AUDIO GROUND RETURNS
AUD_INTMICBIAS
AUD_CODEC_MICBIAS
R6743 2.2K
R6793 3.40K
C6751 4.7UF
GND_AUDIO_CODEC
C6795 0.1UF
AUD_MIC1_IN_P
AUD_MIC_INP_R
C6750 0.0082UF
R6791 100K
C6796 0.1UF
AUD_MIC1_IN_N
AUD_MIC_INN_R
R6792 3.40K
XW6702
AUD_MIC1_IN_G
=PP3V3_S0_AUDIO
R6797 100K
R6798 100K
R6768 100K
R6799 0
AUD_IP_PERPH_DET_DB
AUD_IP_PERIPHERAL_DET
R6796 0
AUD_IP_PERPH_DET_INV
AUD_IP_PERPH_DET_R
Q6703 2N7002
R6700 17.4K
AUD_IP_PER_DEB
Q6701 NTZD3154NT1H
C6797 0.1UF
NOSTUFF
C6740 0.1UF
AUD_IP_PERPH_DET
GND_AUDIO_CODEC
L6738 FERR-250-OHM
=PP12V_S0_AUDIO_SPKRAMP
L6739 FERR-250-OHM
PP12V_AUD_SPKRAMP_PLANE
XW6703
XW6704
GND_AUDIO_SPKRAMP_PLANE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=12V
AUD_SENSE_A
R6790 100K
R6794 20K
AUD_Q6702_D3
NC
Q6702 NTZD3154NT1H
AUD_HP_TYPE
R6795 100K
R6744 39.2K
AUD_Q6701_D6
Q6701 NTZD3154NT1H
AUD_HP_TYPE_INV
R6762 100K
AUD_HP_TIP_DET_INV
AUD_HP_TIP_DET
Q6700 NTZD3154NT1H
R6730 100K
R6732 0
AUD_LI_TIP_DET
AUD_LI_TIP_D
R6701 10K
R6731 0
AUD_LI_TIP_DET_INV
XW6705
R6747 0
R6748 0
R6749 0
SYNC MASTER=SKIPAUDIO
SYNC DATE=06/01/2009
PAGE TITLE
AUDIO: Detects/Grounding
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SIZE D
REVISION A.0.0
BRANCH
PAGE 67 OF 110
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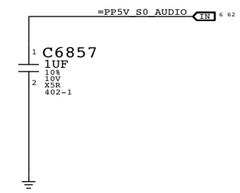
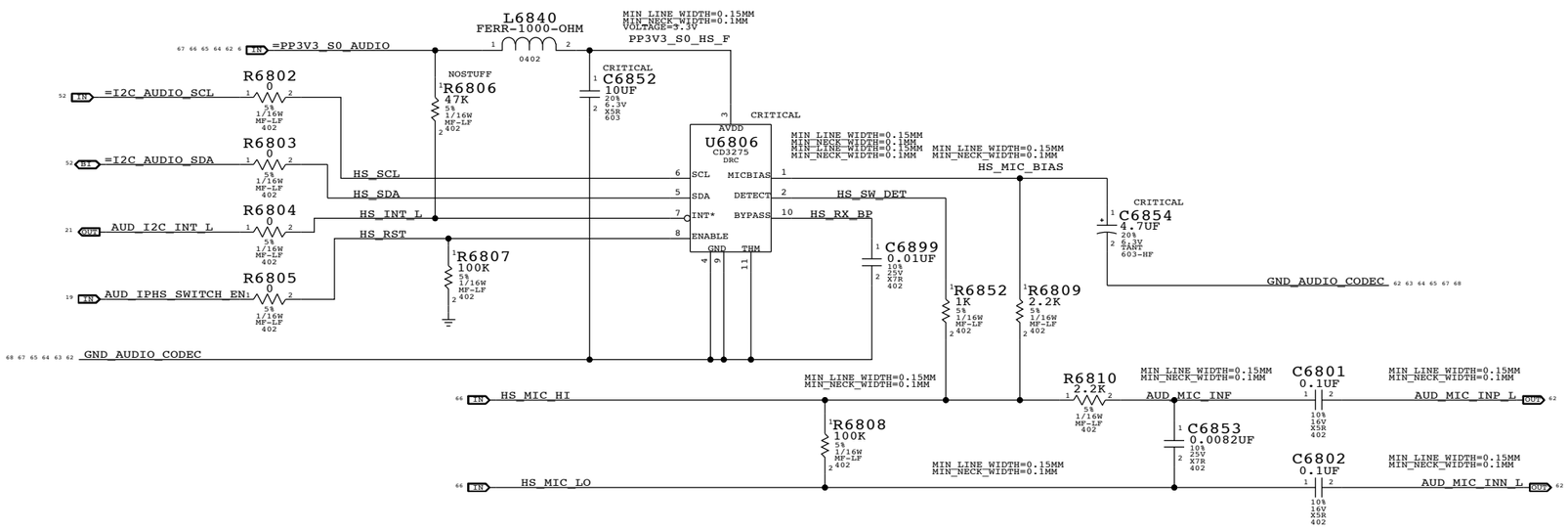
<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

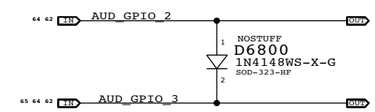
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5



MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256





FLP = 8.82 KHZ
FHP = 80 HZ

SYNC MASTER=SKIPAUDIO SYNC DATE=06/01/2005

PAGE TITLE
AUDIO: Mikey

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S5 POWER RAIL SEQUENCING

12V_S5 — 12V_S5 SUPPLIED BY AC/DC MAX RAMP TIME < 50MS MAX RAMP RATE 10V/MS

3V3_S5 — 3V3_S5 SWITCHER LOGIC POWERED BY INTERAL LDO, SOURCED FROM 12V_S5

1V05_S5 — 1V05_S5 SWITCHER SOURCED FROM 3V3_S5 AND ENABLED FROM 3V3_S5_PGOOD

RMGT POWER RAIL SEQUENCING

MCP: PM_SLP_RMGT_L — PM_SLP_RMGT_L FOLLOWS PM_SLP_S4_L TIMING CLOSELY

3V3_RMGT — 3V3_RMGT FET SOURCED FROM 3V3_S5, ENABLED BY PM_SLP_RMGT_L

1V05_RMGT — 1V05_RMGT FET SOURCED FROM 1V05_S5, ENABLED BY PM_SLP_RMGT_L

S3 POWER RAIL SEQUENCING

MCP: PM_SLP_S4_L

5V3_S3 — 5V_S3 SWITCHER LOGIC POWERED BY INTERNAL LDO (EN BY SLP_S4_L)
OUTPUT SOURCED FROM 12V_S5 AND ENABLED BY PM_SLP_S4_L + LDO OUTPUT GOOD

3V3_S3 — 3V3_S3 FET GATED BY PM_SLP_S4_L

1V5_S3 — 1V5_S3 SWITCHER LOGIC POWERED BY 5V_S3 SO ENABLED BY PGOOD_5V_S3
SOURCED BY 12V_S5; MUST RAMP IN < 2MS

NOTE: NO SEQUENCING REQUIREMENTS FOR THESE 3 RAILS

S0 POWER RAIL SEQUENCING

SB: PM_SLP_S3_L

12V_S0 — 12V_S0 SUPPLIED BY AC/DC, GATED BY PM_SLP_S3_L

5V_S0 — 5V_S0 FET GATED BY PM_SLP_S3_L*12VS0_PG*1V5_S3_PG; RC SOFT TURN-ON CIRCUIT

3V3_S0 — 3V3_S0 FET GATED BY PM_SLP_S3_L*12VS0_PG*1V5_S3_PG; RC SOFT TURN-ON CIRCUIT; SLOWER THAN 5V_S0

1V8_S0 — 1V8_S0 LDO SOURCED FROM 5V_S0, ENABLED BY 5V_S0 WITH RC DELAY

1V5_S0 — 1V5_S0 FET SOURCED FROM 1V5_S3, GATED BY PM_SLP_S3_L*12VS0_PG*1V5_S3_PG WITH RC DELAY

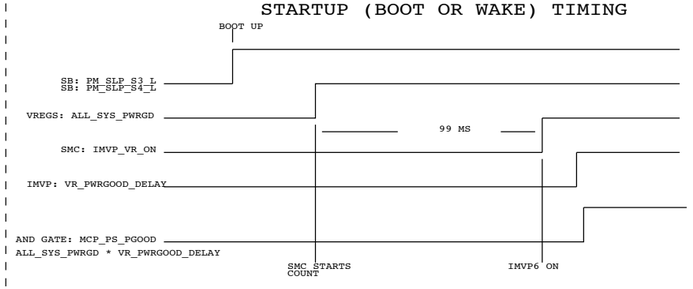
MCP_VCORE — MCP_VCORE REGULATOR INTERNAL LOGIC POWERED FROM 5V_S3, SOURCED FROM 12V_S5,
ENABLED BY PM_SLP_S3_L*12VS0_PG*1V5_S3_PG WITH RC DELAY

1V05_S0 — 1V05_S0 REGULATOR SHARES INTERNAL LOGIC POWER WITH 3V3_S5 REG, SOURCED FROM 12V_S0
ENABLED BY PM_SLP_S3_L*12VS0_PG*1V5_S3_PG WITH RC DELAY

CPU_VCORE

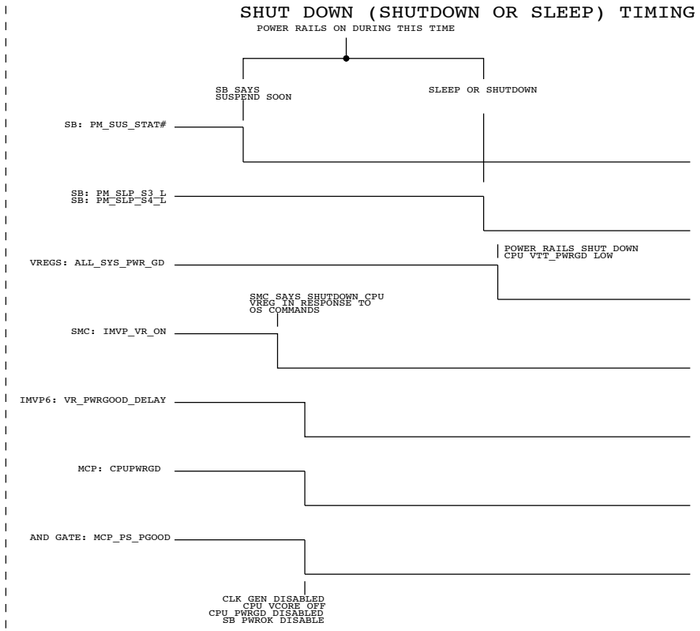
VTT_S0_DDR_LDO

STARTUP (BOOT OR WAKE) TIMING



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



SYNC MASTER=K51 SYNC DATE=12/08/2008

PAGE TITLE
POWER SEQUENCING BLOCK DIAGRAM

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DRAWING NUMBER 051-7845 SIZE D

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PAGE 69 OF 110

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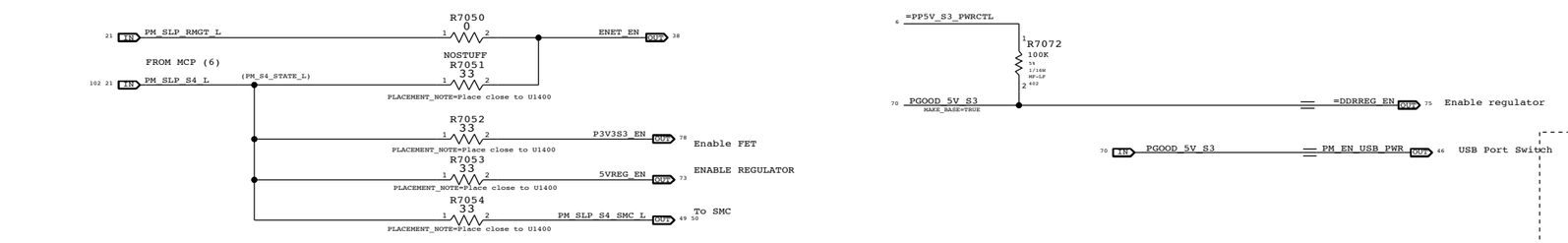
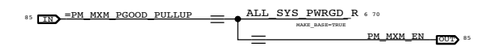
State	SMC_PM_G2_ENABLE (PORTABLES)	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

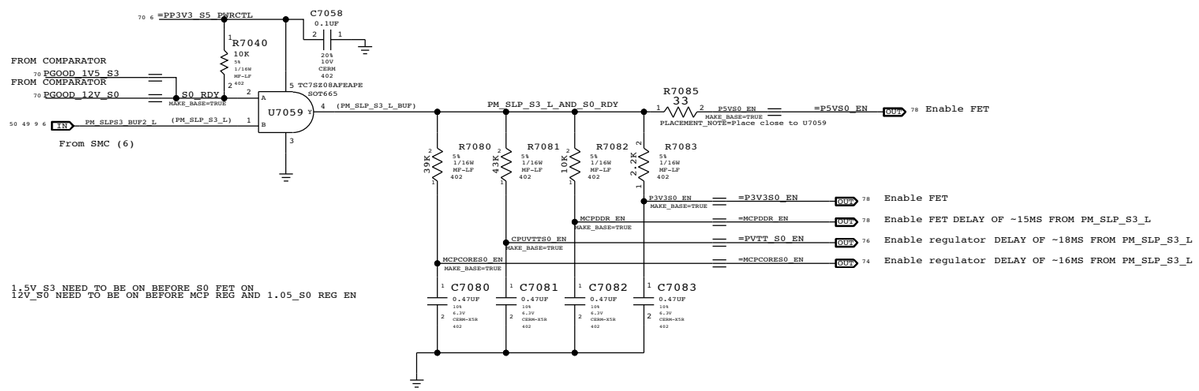
Power Control Signals
3.3V,5V S3 enable



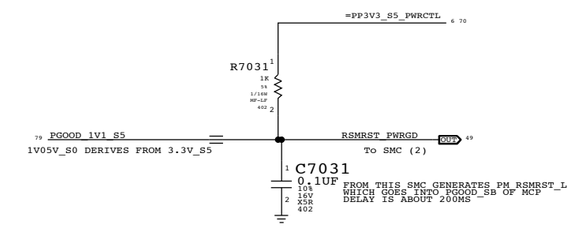
MXM POWER SEQUENCE



MXM CARD INPUT POWER ARE 12V_S0, 3V3_S0, 5V_S0
ALL_SYS_PWRGD ENABLES MXM REGULATORS
PM_MXM_PGOOD IS OPEN DRAIN SIGNAL, IT'S PULLED UP TO ALL_SYS_PWRGD



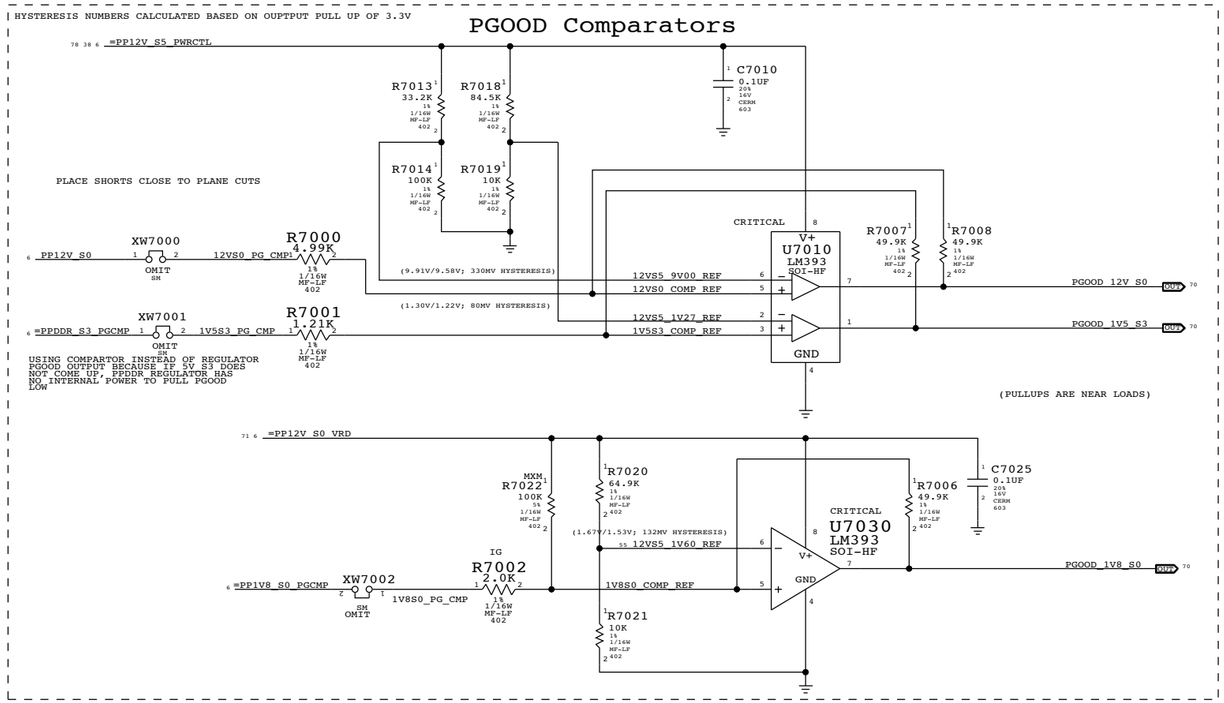
1.5V_S3 NEED TO BE ON BEFORE S0 FET ON
12V_S0 NEED TO BE ON BEFORE MCP REG AND 1.05_S0 REG EN



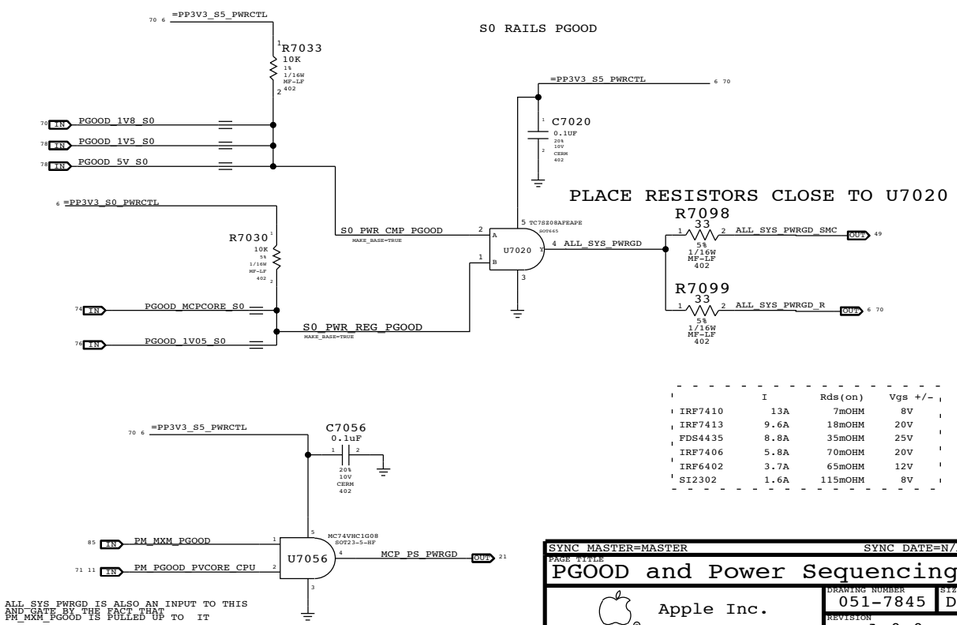
FROM THIS SMC GENERATES PM_RSMRST_L
WHICH GOES INTO PGOOD_SB OF MCP
DELAY IS ABOUT 200MS

PGOOD Comparators

HYSTERESIS NUMBERS CALCULATED BASED ON OUPTPUT PULL UP OF 3.3V



S0 RAILS PGOOD



	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

ALL_SYS_PWRGD IS ALSO AN INPUT TO THIS
AND GATE BY THE FACT THAT
PM_MXM_PGOOD IS PULLED UP TO IT

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
PGOOD and Power Sequencing

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PAGE 70 OF 110
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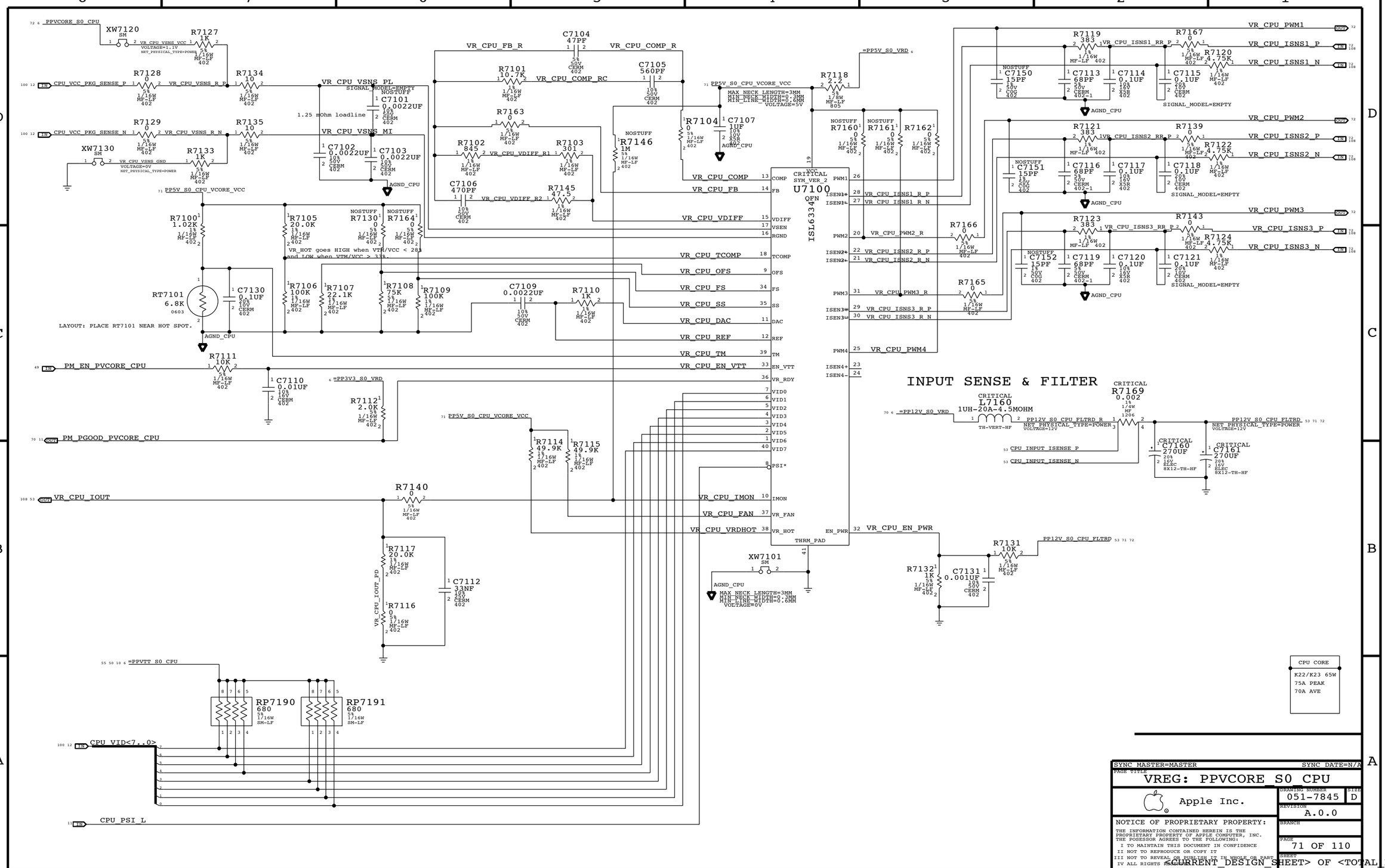

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

VREG: PPVCORE_S0_CPU

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DRAWING NUMBER 051-7845 SIZE D

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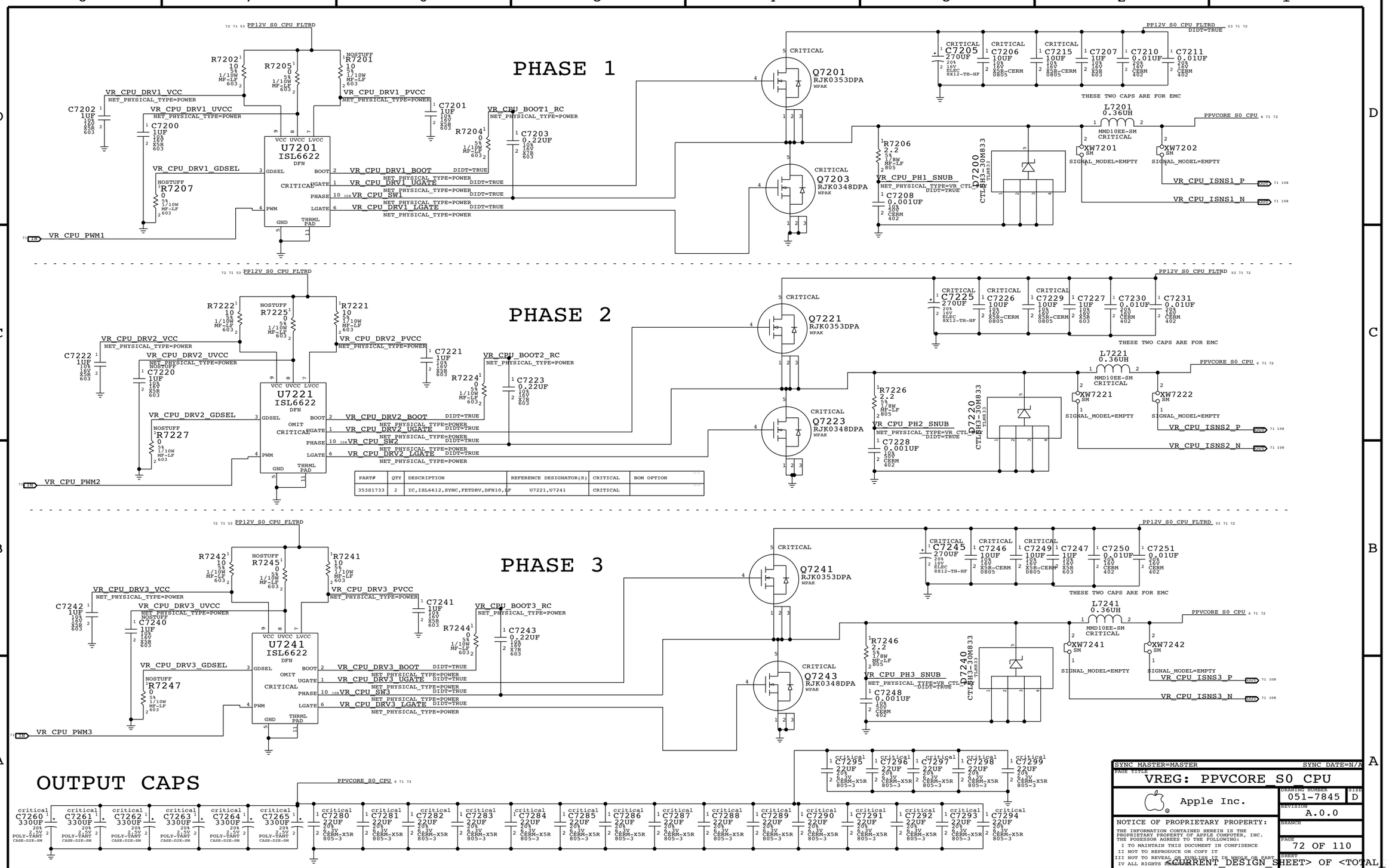

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1733	2	IC,ISL6612,SYNC,FETDRV,DFN10,LF	U7221,U7241	CRITICAL	

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: VREG: PPVCORE_S0_CPU

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DRAWING NUMBER: 051-7845 SIZE: D

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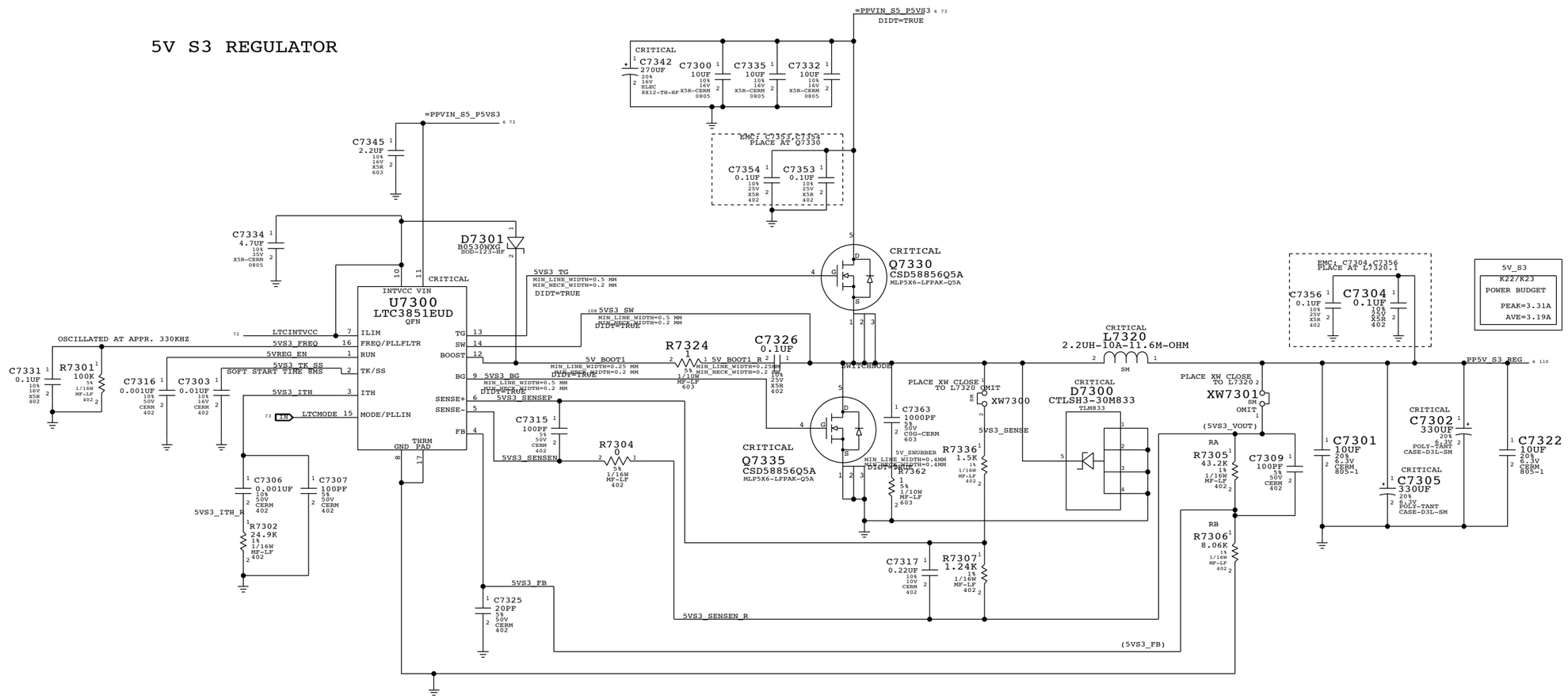
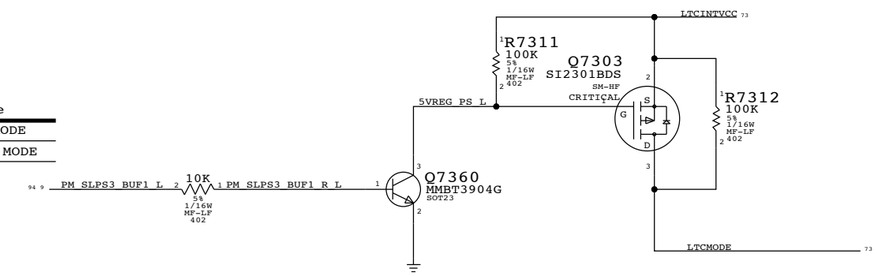
5V S3 REGULATOR



STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: 5V_S3 REGULATOR

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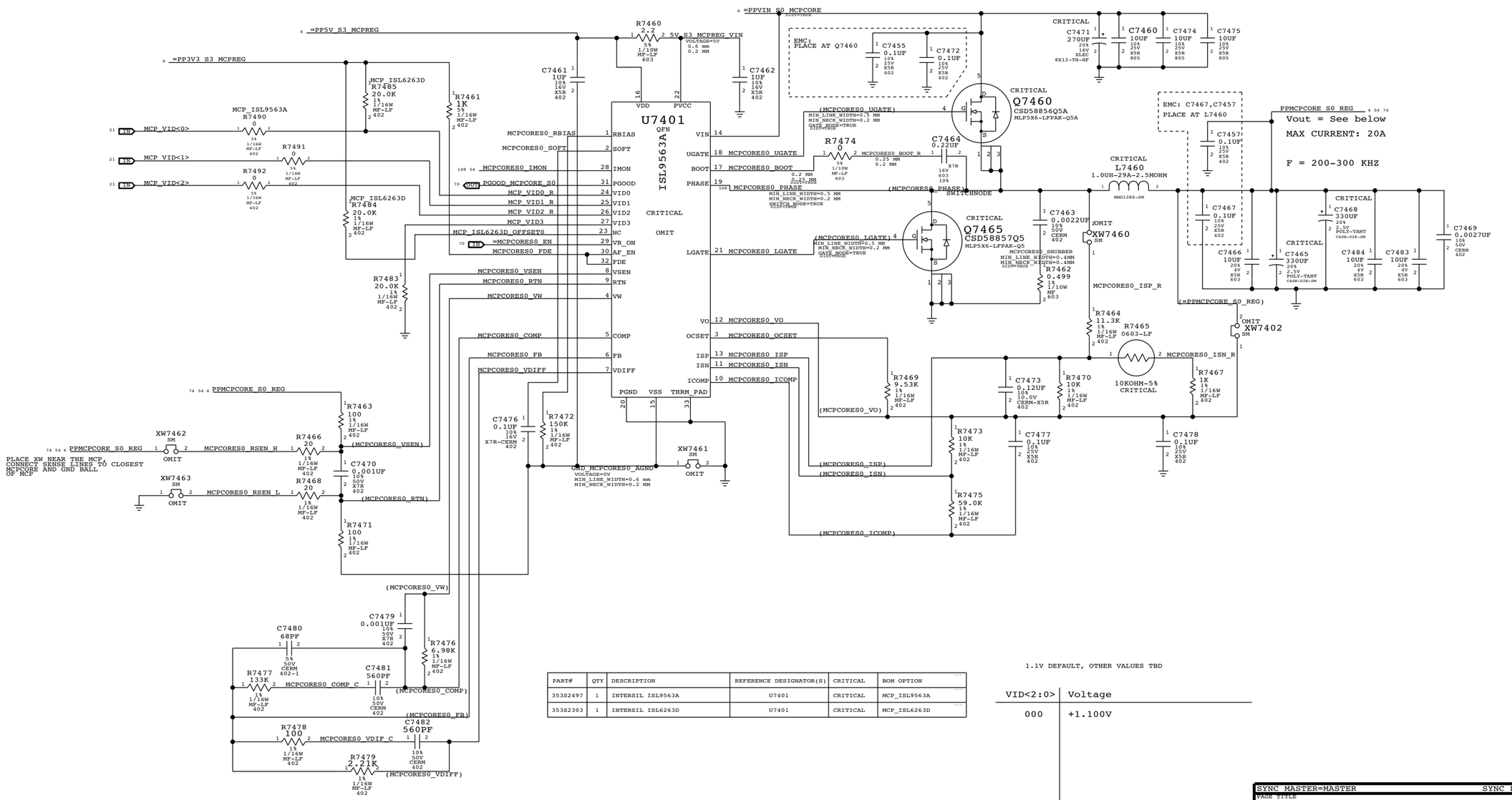
MCP CORE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35382497	1	INTERSIL ISL9563A	U7401	CRITICAL	MCP_ISL9563A
35382303	1	INTERSIL ISL6263D	U7401	CRITICAL	MCP_ISL6263D

1.1V DEFAULT, OTHER VALUES TBD

VID<2:0>	Voltage
000	+1.100V

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: MCP CORE REGULATOR

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DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

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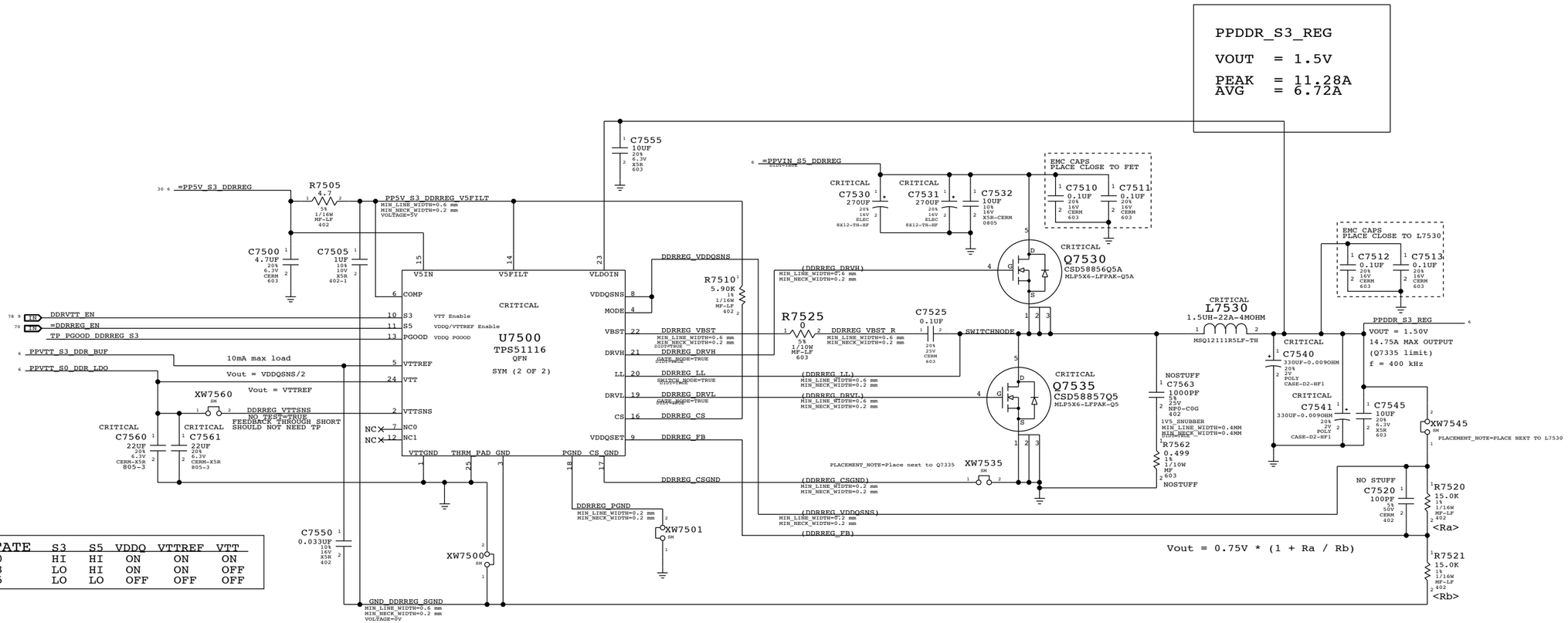
1.5 V DDR SUPPLY



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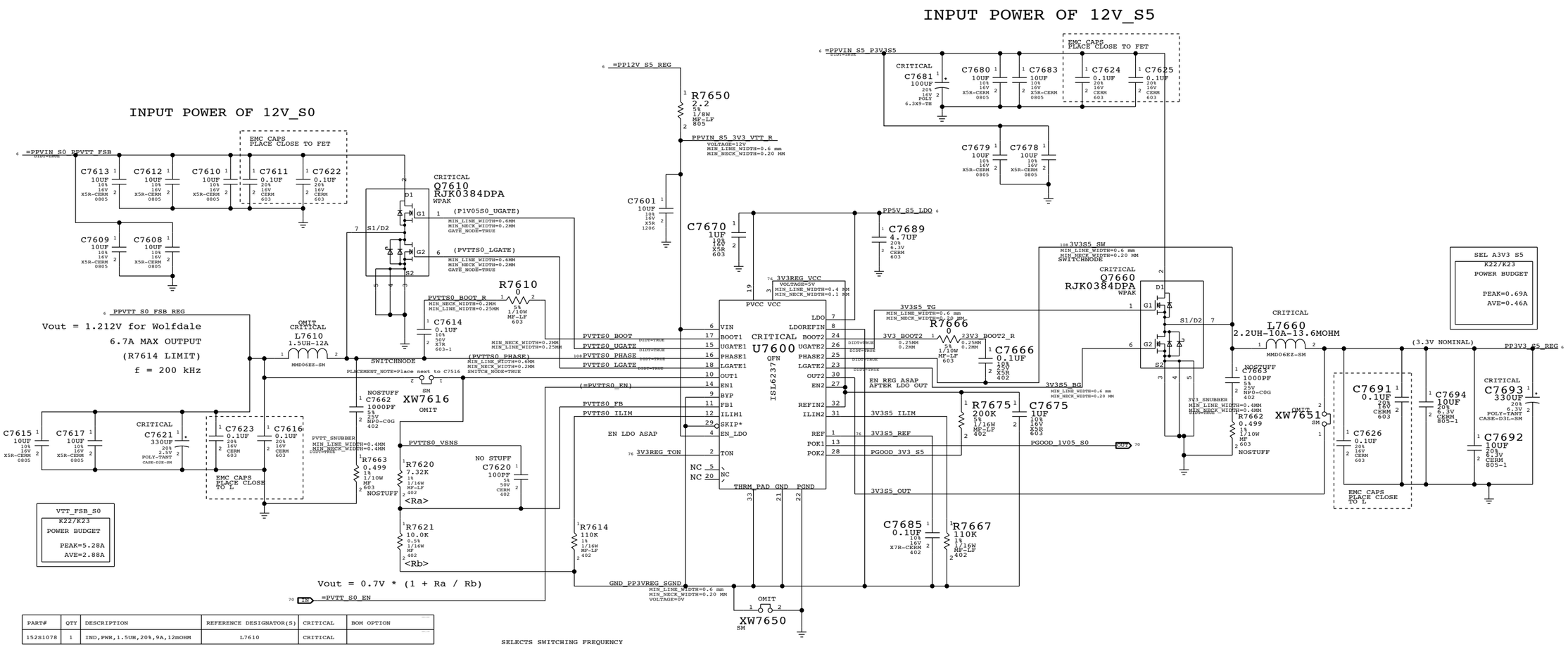
FSB VTT AND 3.3V S5 RAILS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1078	1	IND,PWR,1.5UH,20%,9A,12mOHM	L7610	CRITICAL	

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
FSB VTT/3.3V S5 SUPPLIES

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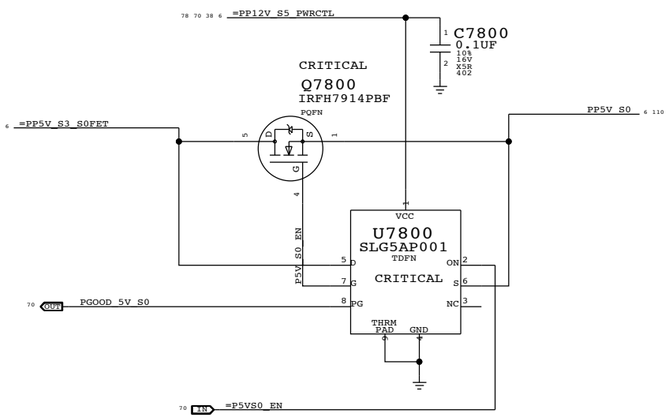
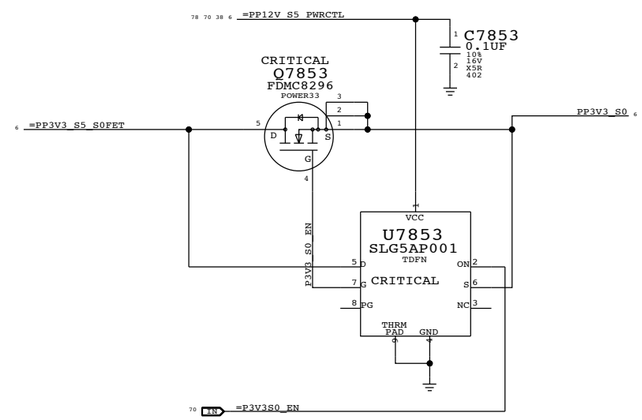
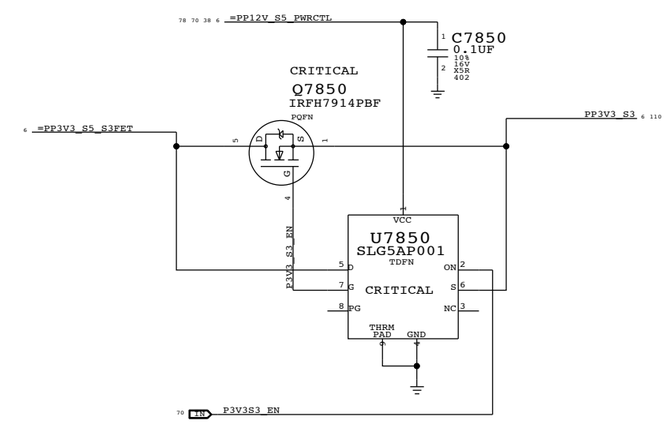
5V S0 FET



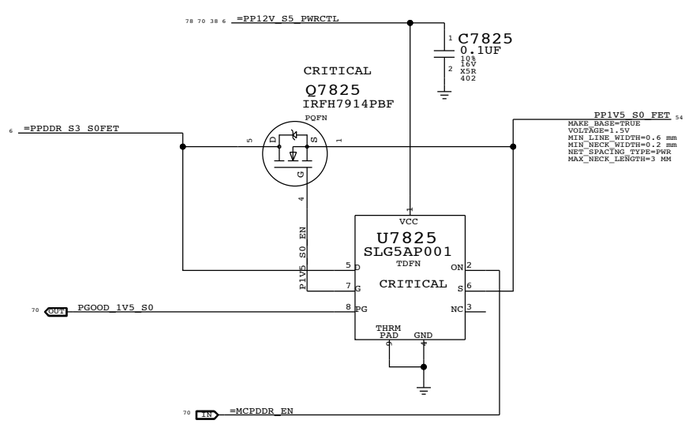
3.3V S0 FET



3.3V S3 FET

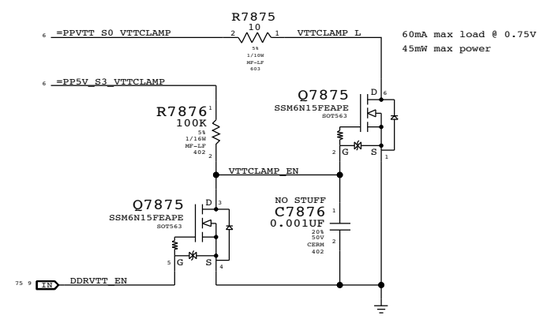


1.5V S0 FET



MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



SYNC MASTER=MASTER	SYNC DATE=N/A
PAGE TITLE: S3 & S0 FETs	
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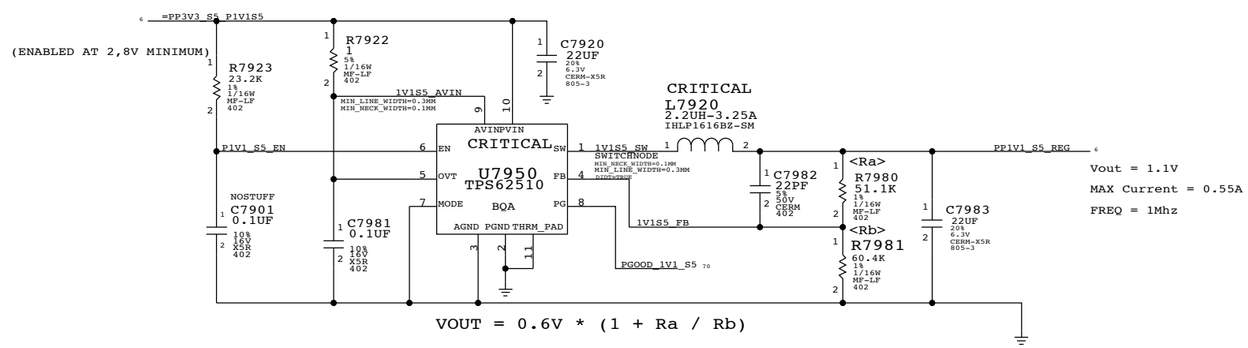
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP 1.1V_S5 AUXC SUPPLY



SYNC MASTER=K51 SYNC DATE=10/31/2008

PAGE TITLE

1V1 S5 POWER SUPPLY

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DRAWING NUMBER 051-7845 SIZE D

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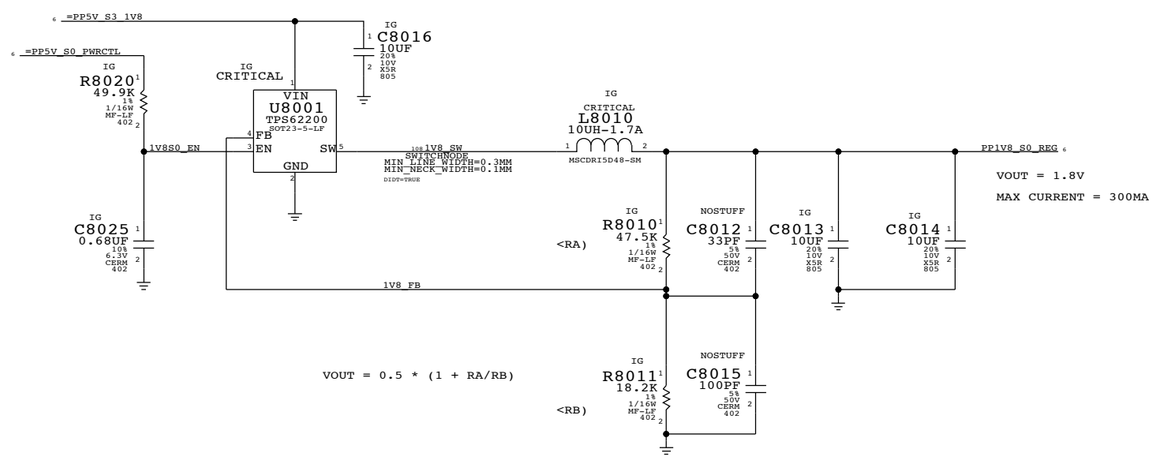
MCP ONLY 1.8V_S0 POWER SUPPLY



SYNC MASTER=MASTER SYNC DATE=N/A

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1V8 POWER SUPPLY

Apple Inc.

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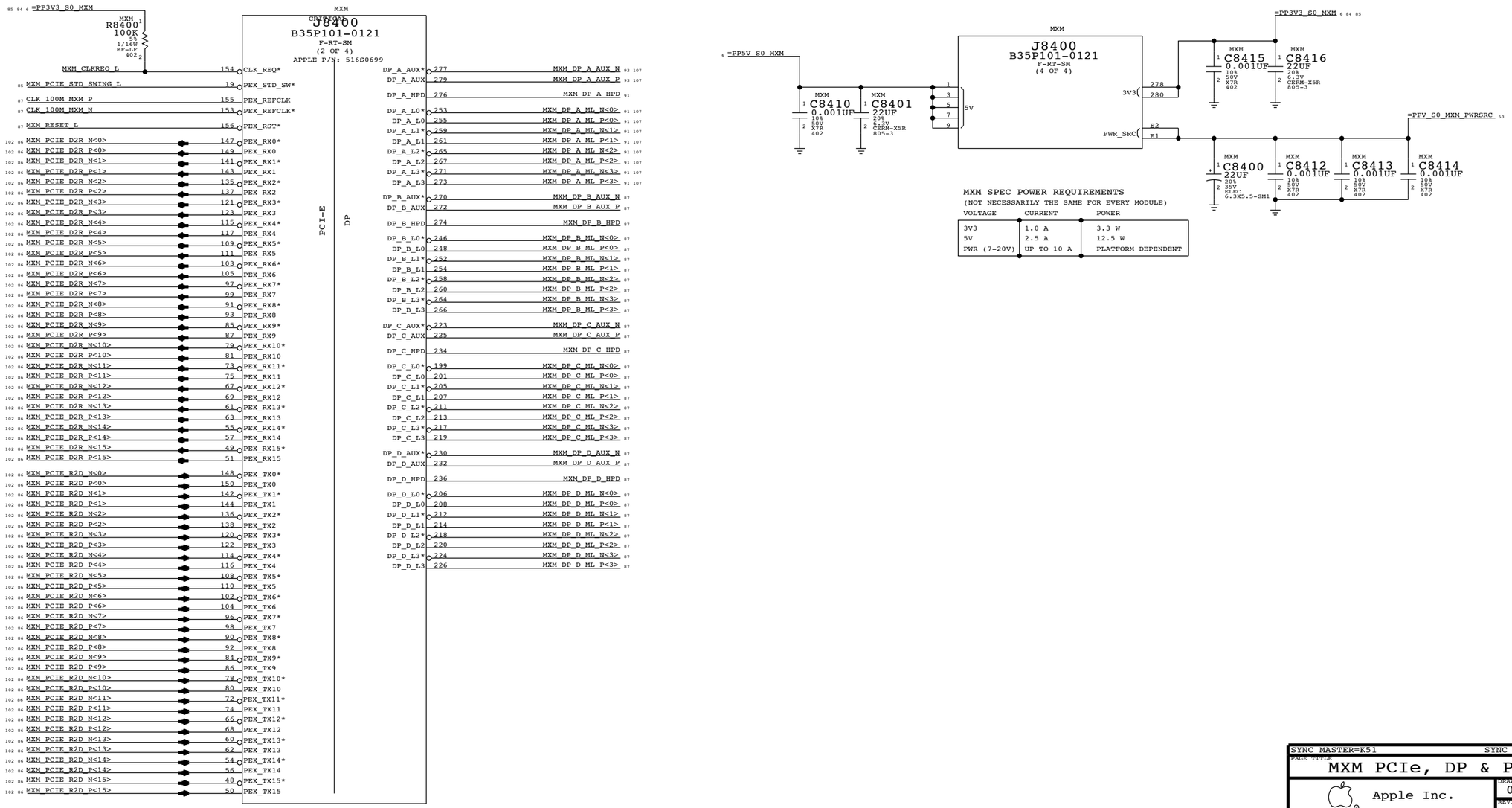
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC MASTER=K51 SYNC DATE=10/31/2008

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

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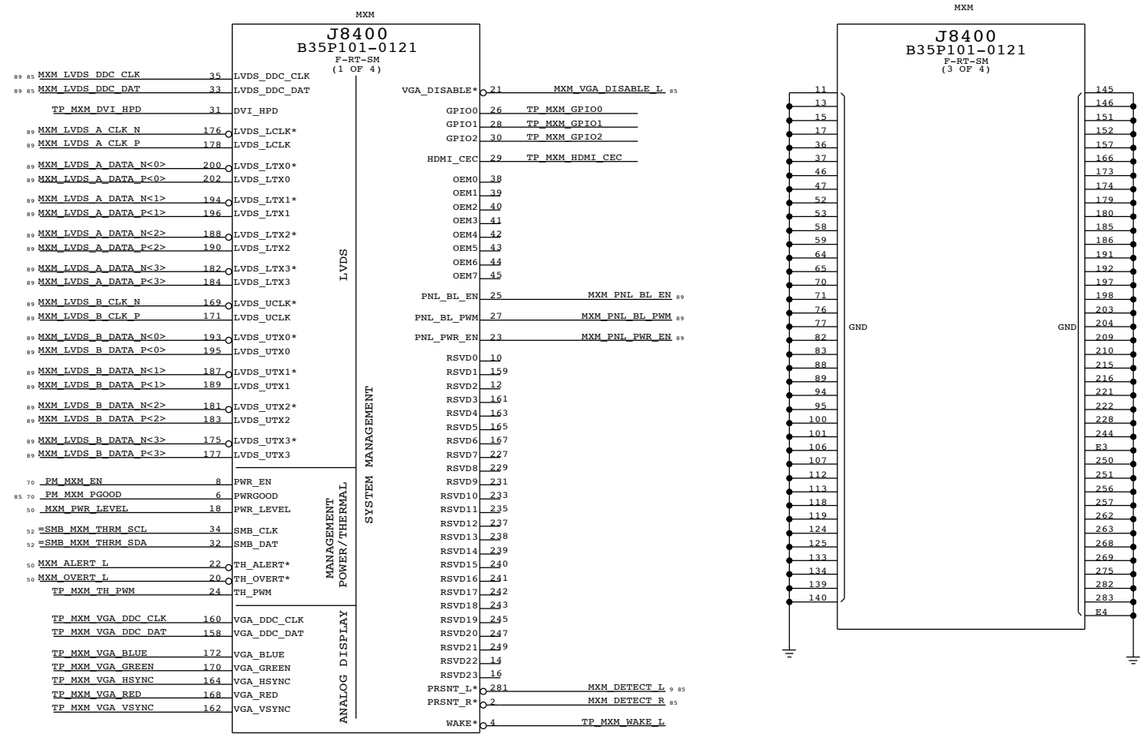
Page Notes

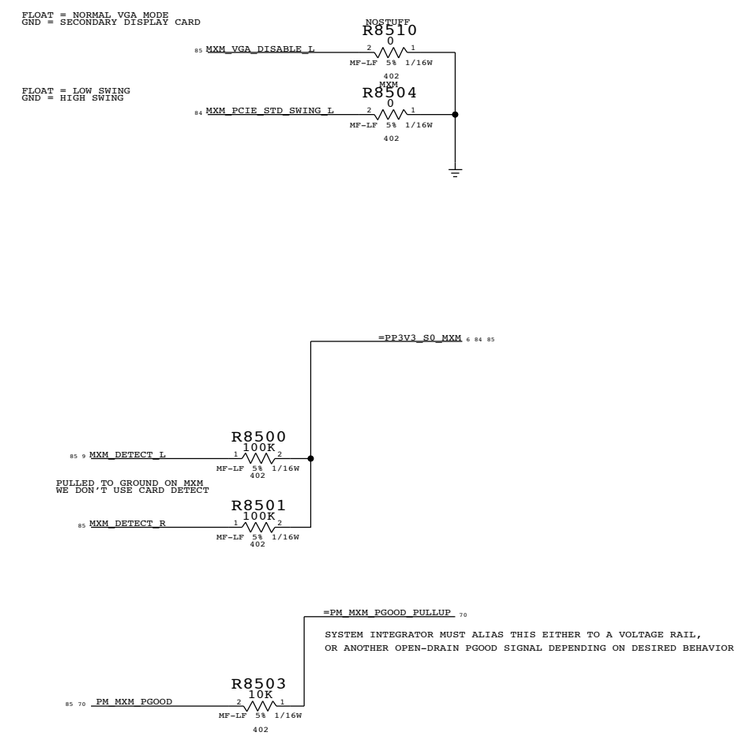
Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

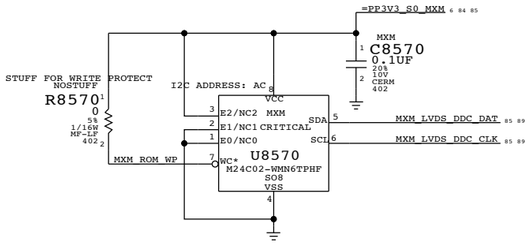
PULLUPS & PULLDOWNS AT MXM CONNECTOR





MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



SYNC MASTER=K51	SYNC DATE=10/31/2008
PAGE TITLE: MXM I/O	
Apple Inc.	DRAWING NUMBER: 051-7845 SIZE: D
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MXM TX CAPS

102 9	IN	PEG_R2D_C_N<0>	MXM C8600 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	OUT	84 102
102 9	IN	PEG_R2D_C_P<0>	MXM C8601 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>	OUT	84 102
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MXM RX CAPS

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102 84	IN	MXM_PCIE_D2R_P<4>	MXM C8654 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<11>	OUT	9 102
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PAGE TITLE
MXM PCIE CAPS

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Page Notes

Power aliases required by this page:
- =PP5V_DP_AUX

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MCP CONNECTIONS

84	CLK_100M_MXM_P	GPU_CLK100M_PCIE_P	MAKE_BASE=TRUE	9 102
84	CLK_100M_MXM_N	GPU_CLK100M_PCIE_N	MAKE_BASE=TRUE	9 102
84	MXM_RESET_L	PEG_RESET_L	MAKE_BASE=TRUE	9 90

UNUSED DP INTERFACES

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84	MXM_DP_C_ML_P<0..3>	NC_MXM_DP_C_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
84	MXM_DP_C_AUX_N	NC_MXM_DP_C_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
84	MXM_DP_C_AUX_P	NC_MXM_DP_C_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
84	MXM_DP_C_HPD	TP_MXM_DP_C_HPD	MAKE_BASE=TRUE
84	MXM_DP_B_ML_N<0..3>	NC_MXM_DP_B_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
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SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
MXM ALIASES

Apple Inc.

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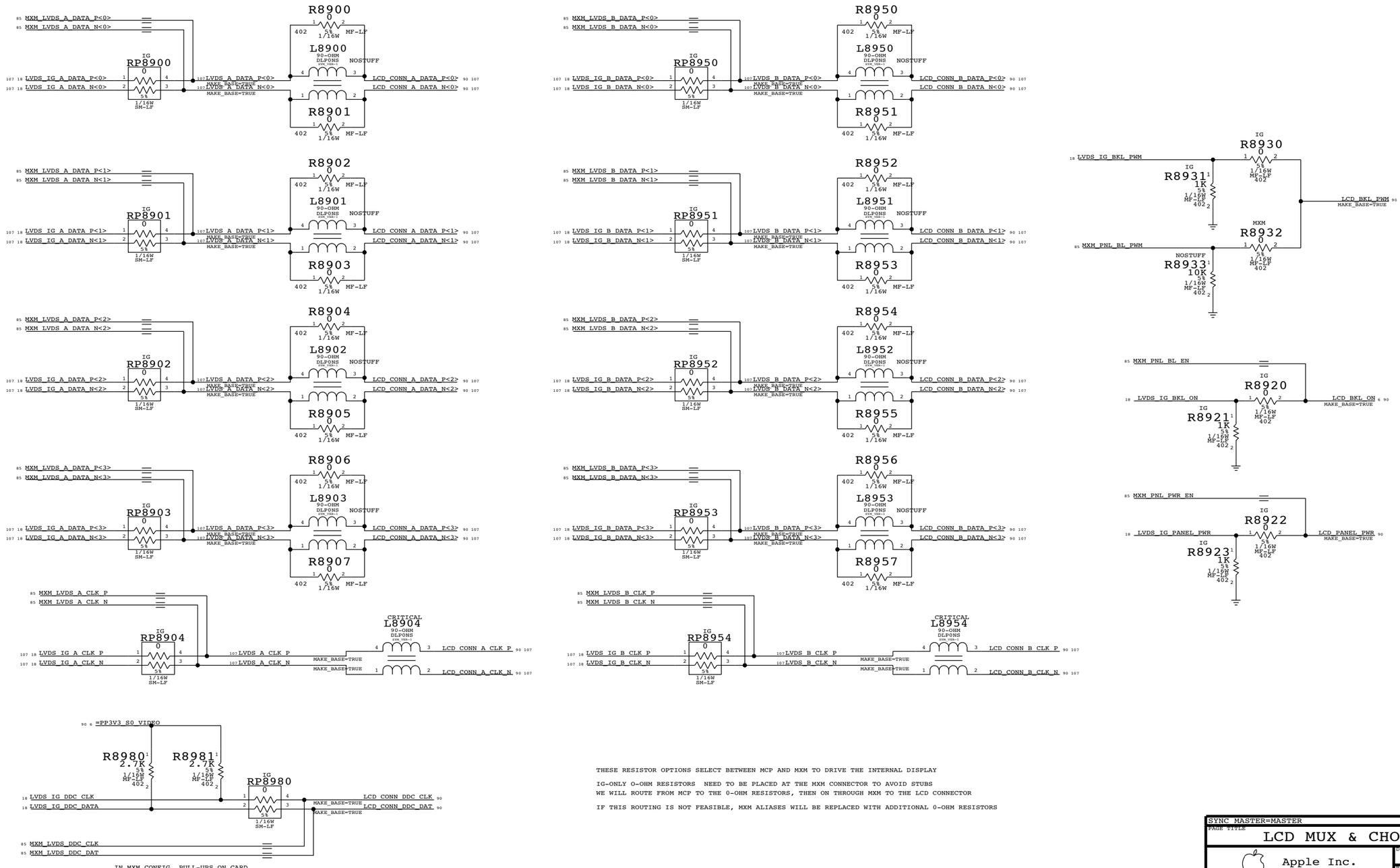
PLACE CHOKES CLOSE TO J9002
SHARE 0-OHM RES WITH CHOKE PADS



IN MXM CONFIG, PULL-UPS ON CARD
IG pullups always stuffed to prevent floating inputs

THESE RESISTOR OPTIONS SELECT BETWEEN MCP AND MXM TO DRIVE THE INTERNAL DISPLAY

IG-ONLY 0-OHM RESISTORS NEED TO BE PLACED AT THE MXM CONNECTOR TO AVOID STUBS
WE WILL ROUTE FROM MCP TO THE 0-OHM RESISTORS, THEN ON THROUGH MXM TO THE LCD CONNECTOR

IF THIS ROUTING IS NOT FEASIBLE, MXM ALIASES WILL BE REPLACED WITH ADDITIONAL 0-OHM RESISTORS

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PAGE TITLE
LCD MUX & CHOKES

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Page Notes

Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

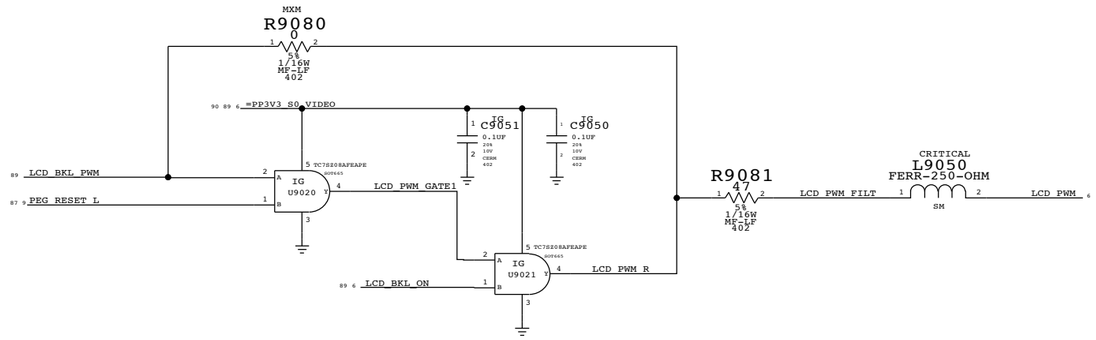
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM

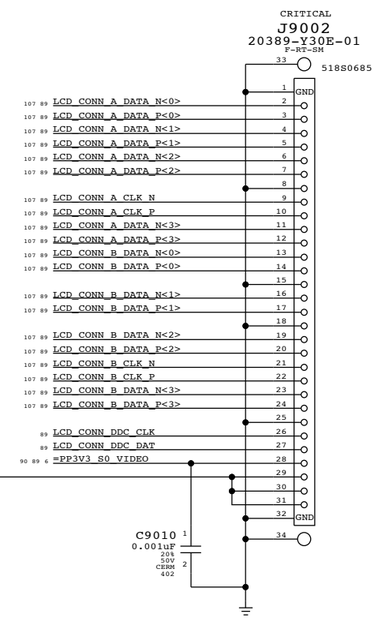
BACKLIGHT CONTROL SUPPORT

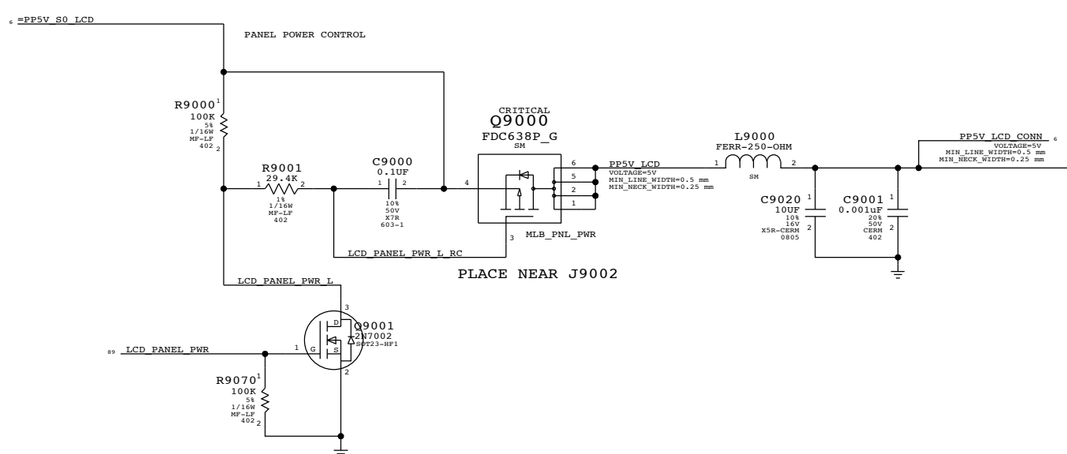
THIS AND GATE CIRCUIT PROVIDES BACKLIGHT GLITCH PREVENTION WHEN MCP GLITCHES GPIOS ON POWERUP
IT MAY BE BYPASSED IF THE PWM SOURCE IS THE MXM

IF NOT BYPASSED, THIS CAN BE USED TO FORCE THE USE OF THE BACKLIGHT ENABLE SIGNAL EVEN IF THE INVERTER DOES NOT TAKE THIS AS AN INPUT



INTERNAL LCD INTERFACE





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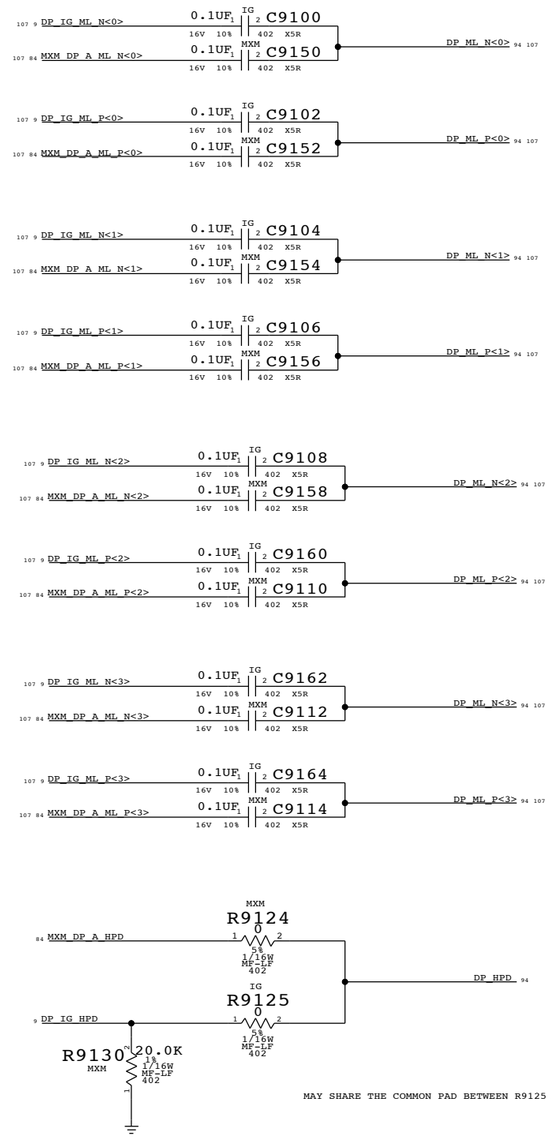
K50 NOTE: PLACE THESE CAPACITORS ATLEAST 1INCH AWAY FROM DP CONNECTOR

DCOX: PLACE AT MXM CONNECTOR IF THERE IS ROOM



MAY SHARE THE COMMON PAD BETWEEN R9125 AND R9130

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DP MUX SUPPORT

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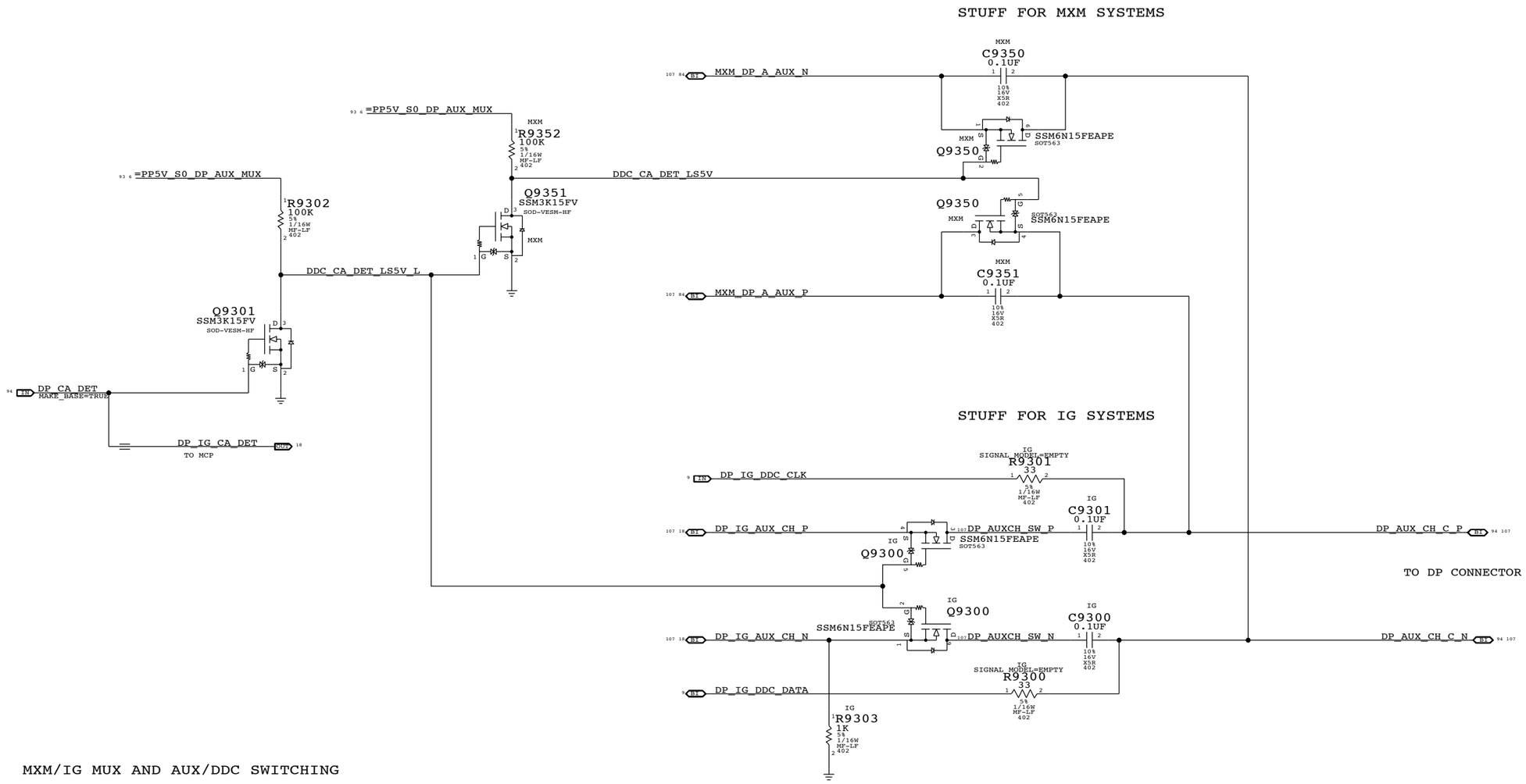

MXM/IG MUX AND AUX/DDC SWITCHING

FOR MXM, Q9350 BYPASSES THE AC COUPLING CAPS
THE CARD IS RESPONSIBLE FOR SWITCHING DDC SIGNALS ONTO THE AUX PAIR

FOR IG SYSTEMS, Q9300 SWITCHES BETWEEN AC COUPLED AUX
AND DC-COUPLED DDC

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DISPLAYPORT SUPPORT

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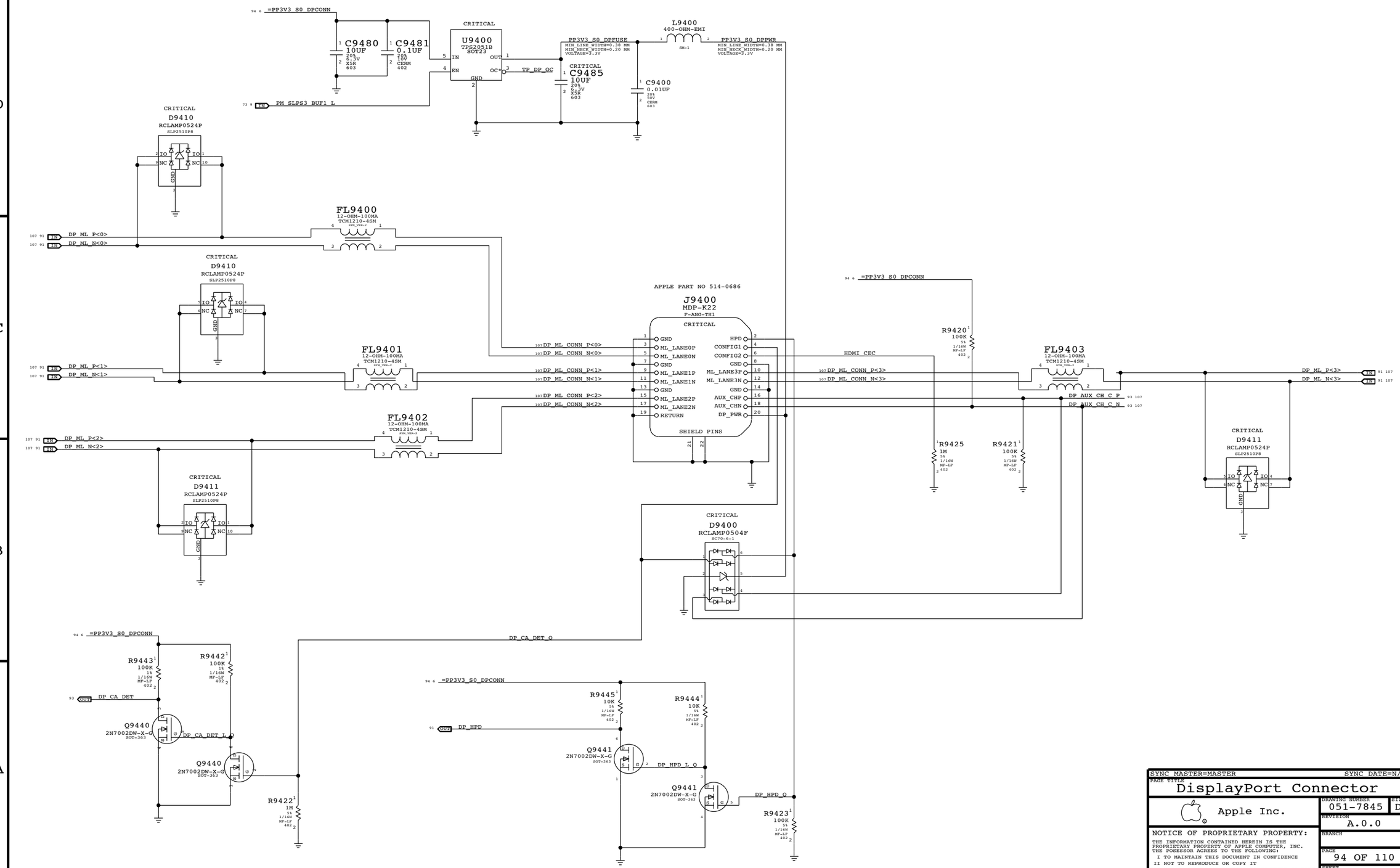

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DisplayPort Connector

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 2x/1x/Async FSB signals with impedance requirements are 50-ohm single-ended.
All 4x FSB signals with impedance requirements are 42-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 90 ps. (Tighther than MCP79)
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_SMIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	Group 0				
		FSB_42S	FSB_DATA	FSB_D_L<15..0>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<0>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
	Group 1				
		FSB_42S	FSB_DATA	FSB_D_L<31..16>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<1>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
	Group 2				
		FSB_42S	FSB_DATA	FSB_D_L<47..32>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<2>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
	Group 3				
		FSB_42S	FSB_DATA	FSB_D_L<63..48>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<3>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB 2X Signals	Group 0				
		FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10 14
		FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
		FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
	Group 1				
		FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10 14
		FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
FSB 1X Signals		FSB_50S	FSB_1X	FSB_ADS_L	10 14
		FSB_50S	FSB_1X	FSB_BREQ0_L	10 14
		FSB_50S	FSB_1X	FSB_BREQ1_L	14
		FSB_50S	FSB_1X	FSB_BNR_L	10 14
		FSB_50S	FSB_1X	FSB_BPRI_L	10 14
		FSB_50S	FSB_1X	FSB_DBSY_L	10 14
		FSB_50S	FSB_1X	FSB_DEFER_L	10 14
		FSB_50S	FSB_1X	FSB_DRDY_L	10 14
		FSB_50S	FSB_1X	FSB_HIT_L	10 14
		FSB_50S	FSB_1X	FSB_HITM_L	10 14
		FSB_50S	FSB_1X	FSB_LOCK_L	10 14
		FSB_50S	FSB_1X	FSB_CPURST_L	10 13 14
		FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
		FSB_50S	FSB_1X	FSB_TRDY_L	10 14
		CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
		CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	11 14
		CPU_50S	CPU_SMIL	CPU_FERR_L	10 14
		CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
		CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
		CPU_50S	CPU_AGTL	CPU_INTR	10 14
		CPU_50S	CPU_AGTL	CPU_NMI	10 14
		CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 14 50
		CPU_50S	CPU_AGTL	CPU_PWRGD	11 13 14
		CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
		CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
		CPU_50S	CPU_SMIL	PM_THRMTRIP_L	11 14 50
		CPU_50S	CPU_AGTL	FSB_CPUSLP_L	11 14
		CPU_50S	CPU_AGTL	CPU_DPSLP_L	11 14
		CPU_50S	CPU_AGTL	CPU_DPRSTP_L	11 14
		MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
		MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
		MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
		MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
		CPU_50S	CPU_AGTL	CPU_IERR_L	10
		CPU_50S	CPU_GTLREF	CPU_GTLREF0	10 11 29
		CPU_50S	CPU_GTLREF	CPU_GTLREF1	10 11 29
		CPU_27P4S	CPU_COMP	CPU_COMP<8>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<3>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<2>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<1>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<0>	11
		CPU_50S	CPU_ITP	CPU_XDP_TDI	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TDO	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TMS	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TCK	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TRST_L	11 13
		CPU_50S	CPU_ITP	CPU_XDP_BPM_L<5..0>	11 13
		CPU_50S	CPU_ITP	CPU_XDP_BPMB<3..0>	11 13
		CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_SMIL	CPU_VID<7..0>	12 71
		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_PKG_SENSE_P	12 71
		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_PKG_SENSE_N	12 71
		CPU_27P4S	CPU_VCCSENSE	VR_CPU_VSNS_R_P	71
		CPU_27P4S	CPU_VCCSENSE	VR_CPU_VSNS_R_N	71

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CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<4..3>	16 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<4..3>	16 33
	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 16 31
	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 16 31
	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 16 31
	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 31
	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<4..3>	16 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<4..3>	16 33
	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 16 32
	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 16 32
	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 16 32
	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 32
	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 33

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 33
	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?
MCP_PEX_COMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE GRAPHICS				
	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 86
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 86
	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 86
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 86
	PCIE_90D	PCIE	MXM_PCIE_R2D_P<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_R2D_N<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_D2R_P<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_D2R_N<15..0>	84 86
PCIE I/O				
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_P	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_N	34
	PCIE_90D	PCIE	PCIE_MINI_D2R_P	17 34
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	17 34
	PCIE_90D	PCIE	PCIE_FW_R2D_P	41
	PCIE_90D	PCIE	PCIE_FW_R2D_N	41
	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 41
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	41
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	41
PCIE REF CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	9 87
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	9 87
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P	34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N	34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 41
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 41
SATA				
	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 45
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 45
	SATA_100D	SATA	SATA_HDD_R2D_P	45 110
	SATA_100D	SATA	SATA_HDD_R2D_N	45 110
	SATA_100D	SATA	SATA_HDD_D2R_P	20 45
	SATA_100D	SATA	SATA_HDD_D2R_N	20 45
	SATA_100D	SATA	SATA_HDD_D2R_C_P	45 110
	SATA_100D	SATA	SATA_HDD_D2R_C_N	45 110
	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 45
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 45
	SATA_100D	SATA	SATA_ODD_R2D_P	45 110
	SATA_100D	SATA	SATA_ODD_R2D_N	45 110
	SATA_100D	SATA	SATA_ODD_D2R_P	20 45
	SATA_100D	SATA	SATA_ODD_D2R_N	20 45
	SATA_100D	SATA	SATA_ODD_D2R_C_P	45 110
	SATA_100D	SATA	SATA_ODD_D2R_C_N	45 110
	MCP_SOS	SATA_TERMP	MCP_SATA_TERMP	20
MISC				
	MCP_SOS	MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
	MCP_DV_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET	18 26
	MCP_SOS	MCP_PEX_COMP	MCP_IFPAB_VPROBE	18 26
			PM_SLP_S3_L	9 21
			PM_SLP_S4_L	21 70

SYNC MASTER=MASTER SYNC DATE=N/A

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_MCP_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

NET_TYPE: ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	PCI_55S	PCI	PCI_REQ0_L	19
	PCI_55S	PCI	PCI_REQ1_L	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
	LPC_55S	LPC	LPC_AD<3..0>	19 49 51
	LPC_55S	LPC	LPC_AD_R<3..0>	19
	LPC_55S	LPC	LPC_FRAME_L	19 49 51
	LPC_55S	LPC	LPC_FRAME_R_L	19
	LPC_55S	LPC	LPC_RESET_L	9 19
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	9 19
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	9 49
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	9 51
	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK_R	9 21
	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK	9 49
	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
	USB_90D	USB	USB_EXTA_P	20 46
	USB_90D	USB	USB_EXTA_N	20 46
	USB_90D	USB	USB_PORT0_P	46
	USB_90D	USB	USB_PORT0_N	46
	USB_90D	USB	USB_EXTB_P	20 46
	USB_90D	USB	USB_EXTB_N	20 46
	USB_90D	USB	USB_PORT1_P	46
	USB_90D	USB	USB_PORT1_N	46
	USB_90D	USB	USB_EXTC_P	20 46
	USB_90D	USB	USB_EXTC_N	20 46
	USB_90D	USB	USB_PORT2_P	46
	USB_90D	USB	USB_PORT2_N	46
	USB_90D	USB	USB_EXTD_P	20 46
	USB_90D	USB	USB_EXTD_N	20 46
	USB_90D	USB	USB_D_MUXED_P	46
	USB_90D	USB	USB_D_MUXED_N	46
	USB_90D	USB	USB_PORT3_P	46
	USB_90D	USB	USB_PORT3_N	46
	USB_90D	USB	USB_CAMERA_P	20 47
	USB_90D	USB	USB_CAMERA_N	20 47
	USB_90D	USB	USB_CAMERA_L_P	47 110
	USB_90D	USB	USB_CAMERA_L_N	47 110
	USB_90D	USB	USB_BT_P	20 47
	USB_90D	USB	USB_BT_N	20 47
	USB_90D	USB	USB_BT_L_P	47 110
	USB_90D	USB	USB_BT_L_N	47 110
	USB_90D	USB	USB_IR_P	20 47
	USB_90D	USB	USB_IR_N	20 47
	USB_90D	USB	USB_IR_L_P	47 110
	USB_90D	USB	USB_IR_L_N	47 110
	USB_90D	USB	USB_SDCARD_P	20 47
	USB_90D	USB	USB_SDCARD_N	20 47
	USB_90D	USB	USB_SDCARD_L_P	47 110
	USB_90D	USB	USB_SDCARD_L_N	47 110
	MCP_50S	SPI	SPI_CLK_R	21 51 61
	MCP_50S	SPI	SPI_CLK	61
	MCP_50S	SPI	SPI_MOSI_R	21 51 61
	MCP_50S	SPI	SPI_MOSI	61
	MCP_50S	SPI	SPI_MISO	21 51 61
	MCP_50S	SPI	SPI_MISO_R	61
	MCP_50S	SPI	SPI_CS0_R_L	21 51
	MCP_50S	SPI	SPI_CS0_L	51
	HDA_55S	HDA	HDA_BIT_CLK	21 62
		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
	HDA_55S	HDA	HDA_BIT_CLK_R	21
	HDA_55S	HDA	HDA_RST_L	21 62
	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_SDOUT	21 62
	HDA_55S	HDA	HDA_SDOUT_R	21
	HDA_55S	HDA	HDA_SYNC	21 62
	HDA_55S	HDA	HDA_SYNC_R	21
	HDA_55S	HDA	HDA_SDIN0	21 62
	HDA_55S	HDA	AUD_SDI_R	62
		HDA	AUD_SPDIF_IN	9 66
		HDA	AUD_SPDIF_OUT	62 66
		HDA	AUD_SPDIF_CHIP	62
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALOUT	21 28
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALIN	21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALOUT	21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALIN	21 28

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MCP_MII_COMP		MCP_MII_COMP_VDD	18
	MCP_MII_COMP		MCP_MII_COMP_GND	18
	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 38
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	37 38
	ENET_MII_55S	ENET_MII	ENET_MDIO	18 37
	ENET_MII_55S	ENET_MII	ENET_MDC	18 37
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 37
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	37
	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 37
	ENET_MII_55S	ENET_MII	ENET_RXD_R<0>	37
	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 37
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..1>	37
	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 37
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	37
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 37
	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 37
	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 37
	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 37
	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	37 39
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	37 39
	ENET_MDI_100D	ENET_MDI	ENET_MDI_T_P<3..0>	39
	ENET_MDI_100D	ENET_MDI	ENET_MDI_T_N<3..0>	39

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FW_110D	FW_TP	FW_PORT0_TPA_P	42 43
	FW_110D	FW_TP	FW_PORT0_TPA_N	42 43
	FW_110D	FW_TP	FW_PORT0_TPB_P	42 43
	FW_110D	FW_TP	FW_PORT0_TPB_N	42 43
PORT 1 & 2 NOT USED				
	FW_110D	FW_TP	FW_P0_TPA_L_P	42
	FW_110D	FW_TP	FW_P0_TPA_L_N	42
	FW_110D	FW_TP	FW_P0_TPB_L_P	42
	FW_110D	FW_TP	FW_P0_TPB_L_N	42

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SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	52
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	52
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	52
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	52
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	52
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	52
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	52
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	52
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	52 106
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	52 106
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	52 106
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	52 106
	SMB_55S	SMB	SMBUS_MCP_0_CLK	13 21 52
	SMB_55S	SMB	SMBUS_MCP_0_DATA	13 21 52

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	0.08 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIspLayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

ELECTRICAL_CONSTRAINT_SET ASSINGED IN CONT. MGR.	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_P<3..0>	84 91
	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_N<3..0>	84 91
	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 91
	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	91 94
	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	91 94
	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	94
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	94
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 93
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 93
	DP_100D	DISPLAYPORT	DP_AUXCH_SW_P	93
	DP_100D	DISPLAYPORT	DP_AUXCH_SW_N	93
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	93 94
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	93 94
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_P	84 93
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_N	84 93
	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 89
	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 89
	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3..0>	18 89
	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3..0>	18 89
	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	18 89
	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	18 89
	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3..0>	18 89
	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3..0>	18 89
	LVDS_100D	LVDS	LVDS_A_DATA_P<3..0>	89
	LVDS_100D	LVDS	LVDS_A_DATA_N<3..0>	89
	LVDS_100D	LVDS	LVDS_B_DATA_P<3..0>	89
	LVDS_100D	LVDS	LVDS_B_DATA_N<3..0>	89
	LVDS_100D	LVDS	LCD_CONN_A_DATA_P<3..0>	89 90
	LVDS_100D	LVDS	LCD_CONN_A_DATA_N<3..0>	89 90
	LVDS_100D	LVDS	LCD_CONN_B_DATA_P<3..0>	89 90
	LVDS_100D	LVDS	LCD_CONN_B_DATA_N<3..0>	89 90
	LVDS_100D	LVDS	LVDS_A_CLK_P	89
	LVDS_100D	LVDS	LVDS_A_CLK_N	89
	LVDS_100D	LVDS	LVDS_B_CLK_P	89
	LVDS_100D	LVDS	LVDS_B_CLK_N	89
	LVDS_100D	LVDS	LCD_CONN_A_CLK_P	89 90
	LVDS_100D	LVDS	LCD_CONN_A_CLK_N	89 90
	LVDS_100D	LVDS	LCD_CONN_B_CLK_P	89 90
	LVDS_100D	LVDS	LCD_CONN_B_CLK_N	89 90
	MCP_DV_COMP		MCP_HDMI_RSET	18 26
	MCP_DV_COMP		MCP_HDMI_VPROBE	18 26

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
AUDIO	*	*	AUDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

K50/K51 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE SPACING		
		PPDDR_MEM	=PP1V5_S3_MEM_A	6 30 31
		PPDDR_MEM	=PP1V5_S3_MEM_B	6 30 32
		SWITCHNODE	VR_CPU_SW1	72
		SWITCHNODE	VR_CPU_SW2	72
		SWITCHNODE	VR_CPU_SW3	72
		SWITCHNODE	1V8_SW	80
		SWITCHNODE	1V1S5_SW	79
		SWITCHNODE	PVTTS0_PHASE	76
		SWITCHNODE	3V3S5_SW	76
		SWITCHNODE	5VS3_SW	73
		SWITCHNODE	MCPCORES0_PHASE	74
	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	55
	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	55
	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	55
	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	55
	THERM_DIFF	THERMAL	CPU_THERMD_P	11 55
	THERM_DIFF	THERMAL	CPU_THERMD_N	11 55
	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	55
	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	55
	THERM_DIFF	THERMAL	MCP_THMDIODE_P	21 55
	THERM_DIFF	THERMAL	MCP_THMDIODE_N	21 55
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_P	53
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_N	53
	THERM_DIFF	THERMAL	SENSE_1V5_S0_P	54
	THERM_DIFF	THERMAL	SENSE_1V5_S0_N	54
	THERM_DIFF	THERMAL	SNS_LCD_P	55 110
	THERM_DIFF	THERMAL	SNS_LCD_N	55 110
	THERM_DIFF	THERMAL	SNS_ODD_P	55 110
	THERM_DIFF	THERMAL	SNS_ODD_N	55 110
	THERM_DIFF	THERMAL	SNS_CPU_H_P	55
	THERM_DIFF	THERMAL	SNS_CPU_H_N	55
	THERM_DIFF	THERMAL	SNS_MCP_P	55
	THERM_DIFF	THERMAL	SNS_MCP_N	55
	THERM_DIFF	THERMAL	SNS_AMB_P	55 110
	THERM_DIFF	THERMAL	SNS_AMB_N	55 110
	THERM_DIFF	THERMAL	SNS_MXM_P	55
	THERM_DIFF	THERMAL	SNS_MXM_N	55
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	71
P23K		THERMAL	SMC_CPU_ISENSE	49 53
P23K		THERMAL	VR_CPU_IOUT	53 71
P23K		THERMAL	VR_ISNS_CPU_P	53
P23K		THERMAL	VR_ISNS_CPU_N	53
P23K		THERMAL	SNS_PS_CPU_ISNS	53
P23K		THERMAL	SMC_CPU_VSENSE	49 53
P23K		THERMAL	CPU_VCC_SENSE	12 53
P23K		THERMAL	SMC_GPU_VSENSE	49 53
P23K		THERMAL	SMC_GPU_ISENSE	49 53
P23K		THERMAL	SMC_1V5_S0_ISENSE	50 54
P23K		THERMAL	SMC_1V5_S0_ISENSE_R	54
P23K		THERMAL	SMC_1V5_S0_VSENSE	50 54
P23K		THERMAL	SMC_MCP_CORE_ISENSE	50 54
P23K		THERMAL	SMC_MCP_CORE_VSENSE	50 54
P23K		THERMAL	MCPCORES0_IMON	54 74
P23K		THERMAL	CPU_PECI_L	11 55
P23K		THERMAL	SMB_PECI_L	55
P23K		THERMAL	CPU_PECI_MCP	14 55
		THERMAL	HDD_OOB_TEMP_FILT	55
P23K		THERMAL	HDD_OOB_TEMP	55
P23K		THERMAL	HDD_OOB_TEMP_R	55
P23K		THERMAL	SMC_HDD_OOB_TEMP	55

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K22/K23 SPECIFIC CONSTRAINTS

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K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.300 MM	0.085 MM	=STANDARD		
27P4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP,BOTTOM	Y	0.151 MM	0.085 MM	=STANDARD		
42_OHM_SE	*	Y	0.136 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	*	POWER_WIDTH
VR_CTL_PHY	*	POWER_WIDTH

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM

CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI,LPC,SMB,HDA,SPI,RGMII,SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

103 47	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
103 47	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

103 47	IN	USB_SDCARD_L_P	FUNC_TEST=TRUE
103 47	IN	USB_SDCARD_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

103 47	IN	USB_BT_L_P	FUNC_TEST=TRUE
103 47	IN	USB_BT_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

103 47	IN	USB_IR_L_P	FUNC_TEST=TRUE
103 47	IN	USB_IR_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

102 45	IN	SATA_ODD_R2D_P	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_R2D_N	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_D2R_C_N	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_D2R_C_P	FUNC_TEST=TRUE
49 45	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

102 45	IN	SATA_HDD_R2D_P	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_R2D_N	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_D2R_C_N	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_D2R_C_P	FUNC_TEST=TRUE

3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

108 55	IN	SNS_LCD_P	FUNC_TEST=TRUE
108 55	IN	SNS_LCD_N	FUNC_TEST=TRUE

J5521 AMBIENT TEMP SENSOR

108 55	IN	SNS_AMB_P	FUNC_TEST=TRUE
108 55	IN	SNS_AMB_N	FUNC_TEST=TRUE

J5551 ODD TEMP SENSOR

108 55	IN	SNS_ODD_P	FUNC_TEST=TRUE
108 55	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

56	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
56	IN	FAN_TACH0_L	FUNC_TEST=TRUE
56	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
56	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

57	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
57	IN	FAN_TACH2_L	FUNC_TEST=TRUE
57	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
57	IN	FAN_2_GND	FUNC_TEST=TRUE

J5601 HD FAN

56	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
56	IN	FAN_TACH1_L	FUNC_TEST=TRUE
56	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
56	IN	FAN_1_GND	FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

66	IN	AUD_MIC_IN1_N_CONN	FUNC_TEST=TRUE
66	IN	GND_AUDIO_MIC1_CONN	FUNC_TEST=TRUE
66	IN	AUD_MIC_IN1_P_CONN	FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

	IN	AUD_SPKR_OUTLO2R_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO2R_N	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1R_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1R_N	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

	IN	AUD_SPKR_OUTLO2L_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO2L_N	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1L_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1L_N	FUNC_TEST=TRUE

		GND	16 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=16
78 6	IN	PP3V3_S3	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
73 6	IN	PP5V_S3_REG	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
78 6	IN	PP5V_S0	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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